ECE 213 – Digital Electronics

100 Hard & Concept-Wise MCQs with Answers and Solutions

Number Systems & Codes

Q1. The decimal equivalent of (110101.101)■ is:

A) 53.625

B) 53.5

C) 54.625

D) 52.625

Answer: A) 53.625
Solution: 110101■ = 53 and .101■ = 0.625, so the result is 53.625.

Q2. The 8-bit 2's complement representation of -37 is:

A) 11011011

B) 11011010

C) 10110101

D) 11011101

Answer: A) 11011011
Solution: 37 = 00100101; invert and add 1 to get 11011011.

Q3. Which code changes only one bit between two consecutive code words?

A) BCD

B) Excess-3

C) Gray

D) ASCII

Answer: C) Gray
Solution: Gray code is a unit-distance code.

Q4. The Excess-3 representation of decimal 7 is:

A) 0111

B) 1001

C) 1010

D) 1011

Answer: C) 1010
Solution: 7 + 3 = 10, whose binary form is 1010.

Q5. Which of the following is an invalid BCD code?

A) 0101

B) 1001

C) 1010

D) 0011

Answer: C) 1010
Solution: BCD represents decimal digits 0 through 9; 1010 represents 10.

Boolean Algebra & Logic Gates

Q6. Simplify: F = A + AB

A) A

B) B

C) AB

D) A+B

Answer: A) A
Solution: By the absorption law, A + AB = A.

Q7. According to De Morgan's theorem, (AB)' equals:

A) A'B'

B) A' + B'

C) A+B

D) AB

Answer: B) A' + B'
Solution: The complement of a product is the sum of the complements.

Q8. Which pair consists entirely of universal gates?

A) AND and OR

B) XOR and XNOR

C) NAND and NOR

D) NOT and XOR

Answer: C) NAND and NOR
Solution: NAND and NOR can implement any Boolean function.

Q9. If A=1 and B=0, the output of A XNOR B is:

A) 0

B) 1

C) X

D) Z

Answer: A) 0
Solution: XNOR is 1 only when the inputs are equal.

Q10. The Boolean expression A'B + AB' represents:

A) AND

B) OR

C) XOR

D) XNOR

Answer: C) XOR
Solution: This is the standard XOR expression.

SOP, POS & Minterms

Q11. The canonical SOP form of a Boolean function is expressed using:

A) Maxterms

B) Minterms

C) Literals only

D) Don't-care terms only

Answer: B) Minterms
Solution: Canonical SOP is a sum of minterms.

Q12. The canonical POS form is represented by:

A) Σ

B) Π

C) Δ

D) λ

Answer: B) Π
Solution: Product of maxterms is represented by Π notation.

Q13. For a 3-variable Boolean function, the total number of possible minterms is:

A) 3

B) 6

C) 8

D) 9

Answer: C) 8
Solution: There are $2^3 = 8$ minterms.

Q14. The minterm corresponding to A=1, B=0, C=1 is:

A) A'BC

B) AB'C

C) ABC'

D) A'B'C

Answer: B) AB'C
Solution: A=1, B=0, C=1 gives AB'C.

Q15. In a K-map, SOP minimization is performed by grouping:

A) 0s

B) 1s

C) X only

D) 0s and 1s equally

Answer: B) 1s
Solution: SOP minimization groups 1s.

K-Map

Q16. A 4-variable K-map contains:

A) 4 cells

B) 8 cells

C) 16 cells

D) 32 cells

Answer: C) 16 cells
Solution: 2■ = 16 cells.

Q17. A valid K-map group can contain:

A) 3 cells

B) 5 cells

C) 6 cells

D) 8 cells

Answer: D) 8 cells
Solution: Valid groups contain powers of two cells.

Q18. A group of 4 cells in a 4-variable K-map eliminates:

A) 1 variable

B) 2 variables

C) 3 variables

D) 4 variables

Answer: B) 2 variables
Solution: A group of 4 eliminates two variables.

Q19. Don't-care conditions are generally represented by:

A) Z

B) X

C) Y

D) D

Answer: B) X
Solution: X is commonly used for don't-care conditions.

Q20. In K-map simplification, opposite edges are considered:

A) Non-adjacent

B) Adjacent

C) Invalid

D) Independent

Answer: B) Adjacent
Solution: K-map edges wrap around and are adjacent.

Adders & Subtractors

Q21. The Sum output of a half adder is:

A) AB

B) A+B

C) A XOR B

D) A XNOR B

Answer: C) A XOR B
Solution: Sum = A XOR B.

Q22. The Carry output of a half adder is:

A) A+B

B) AB

C) A XOR B

D) A'B

Answer: B) AB
Solution: Carry = AB.

Q23. A full adder has:

A) 2 inputs and 1 output

B) 3 inputs and 2 outputs

C) 2 inputs and 2 outputs

D) 3 inputs and 1 output

Answer: B) 3 inputs and 2 outputs
Solution: Inputs are A, B and Cin; outputs are Sum and Carry.

Q24. For a full adder with A=1, B=1 and Cin=1, the outputs are:

A) Sum=0, Carry=0

B) Sum=1, Carry=1

C) Sum=1, Carry=0

D) Sum=0, Carry=1

Answer: B) Sum=1, Carry=1
Solution: 1+1+1 = binary 11.

Q25. A full adder can be constructed using:

A) Two half adders and an OR gate

B) Two OR gates only

C) One half adder only

D) Two decoders

Answer: A) Two half adders and an OR gate
Solution: Two half adders plus an OR gate implement a full adder.

Comparator

Q26. The Difference output of a half subtractor is:

A) AB

B) A+B

C) A XOR B

D) A'B

Answer: C) A XOR B
Solution: Difference = A XOR B.

Q27. The Borrow output of a half subtractor is:

A) AB

B) A'B

C) AB'

D) A+B

Answer: B) A'B
Solution: Borrow = A'B.

Q28. A full subtractor has:

A) 2 inputs

B) 3 inputs

C) 4 inputs

D) 5 inputs

Answer: B) 3 inputs
Solution: Inputs are A, B and borrow-in.

Q29. A magnitude comparator determines:

A) Only A>B

B) Only A<B

C) A>B, A=B and A<B

D) Only A=B

Answer: C) A>B, A=B and A<B
Solution: A comparator provides all three magnitude relationships.

Q30. Which circuit is used to compare two binary numbers?

A) Encoder

B) Comparator

C) Decoder

D) Register

Answer: B) Comparator
Solution: A magnitude comparator compares binary numbers.

Multiplexer

Q31. A 4-to-1 multiplexer requires:

A) 1 select line

B) 2 select lines

C) 3 select lines

D) 4 select lines

Answer: B) 2 select lines
Solution: 2 select lines select one of 4 inputs.

Q32. An 8-to-1 multiplexer requires:

A) 2 select lines

B) 3 select lines

C) 4 select lines

D) 8 select lines

Answer: B) 3 select lines
Solution: $2^3 = 8$, so 3 select lines are required.

Q33. A 16-to-1 multiplexer requires:

A) 2 select lines

B) 3 select lines

C) 4 select lines

D) 5 select lines

Answer: C) 4 select lines
Solution: 2■ = 16.

Q34. A multiplexer is also known as:

A) Data distributor

B) Data selector

C) Data encoder

D) Data comparator

Answer: B) Data selector
Solution: A MUX selects one of many inputs.

Q35. A multiplexer can be used to implement:

A) Boolean functions

B) Memory cells only

C) Counters only

D) Flip-flops only

Answer: A) Boolean functions
Solution: MUXes can implement Boolean functions.

DEMUX, Encoder & Decoder

Q36. A 1-to-8 DEMUX requires:

A) 2 select lines

B) 3 select lines

C) 4 select lines

D) 8 select lines

Answer: B) 3 select lines
Solution: Three select lines choose one of eight outputs.

Q37. A DEMUX is also known as:

A) Data selector

B) Data distributor

C) Code converter

D) Comparator

Answer: B) Data distributor
Solution: A DEMUX distributes one input to a selected output.

Q38. A 3-to-8 decoder has:

A) 3 outputs

B) 6 outputs

C) 8 outputs

D) 16 outputs

Answer: C) 8 outputs
Solution: $2^3 = 8$ outputs.

Q39. An 8-to-3 encoder has:

A) 3 inputs and 8 outputs

B) 8 inputs and 3 outputs

C) 8 inputs and 8 outputs

D) 3 inputs and 3 outputs

Answer: B) 8 inputs and 3 outputs
Solution: An encoder converts one of 8 inputs into a 3-bit code.

Q40. A priority encoder is useful when:

A) No input is active

B) More than one input may be active

C) Only analog signals are present

D) No output is required

Answer: B) More than one input may be active
Solution: Priority encoders resolve multiple active inputs.

Latches

Q41. A latch is generally:

A) Edge-sensitive

B) Level-sensitive

C) Frequency-sensitive

D) Analog

Answer: B) Level-sensitive
Solution: Latches are level-sensitive storage elements.

Q42. In an SR latch, S stands for:

A) Shift

B) Set

C) Serial

D) Select

Answer: B) Set
Solution: S means Set.

Q43. In an SR latch, R stands for:

A) Read

B) Register

C) Reset

D) Rotate

Answer: C) Reset
Solution: R means Reset.

Q44. The forbidden input condition for a basic NOR SR latch is:

A) S=0,R=0

B) S=1,R=0

C) S=0,R=1

D) S=1,R=1

Answer: D) S=1,R=1
Solution: S=R=1 is the invalid condition for a NOR SR latch.

Q45. A D latch is designed mainly to eliminate:

A) Clock signal

B) Invalid SR condition

C) Data input

D) Output

Answer: B) Invalid SR condition
Solution: The D arrangement avoids the invalid SR combination.

Flip-Flops

Q46. A flip-flop can store:

A) 1 bit

B) 2 bits

C) 4 bits

D) 8 bits

Answer: A) 1 bit
Solution: A flip-flop stores one bit.

Q47. A JK flip-flop with J=K=1 performs:

A) Set

B) Reset

C) Toggle

D) Hold

Answer: C) Toggle
Solution: J=K=1 causes toggling.

Q48. A JK flip-flop with J=0 and K=0 performs:

A) Set

B) Reset

C) Toggle

D) No change

Answer: D) No change
Solution: J=K=0 means hold.

Q49. A T flip-flop with T=1:

A) Holds

B) Toggles

C) Resets

D) Sets only

Answer: B) Toggles
Solution: T=1 toggles the output.

Q50. The primary advantage of a D flip-flop is:

A) It has no clock

B) It eliminates the invalid SR state

C) It cannot store data

D) It requires four inputs

Answer: B) It eliminates the invalid SR state
Solution: D flip-flop has a single data input and avoids the invalid SR condition.

Flip-Flop Timing

Q51. Race-around condition occurs in a JK flip-flop when:

A) J=0,K=0

B) J=1,K=0

C) J=0,K=1

D) J=1,K=1 with a long clock pulse

Answer: D) J=1,K=1 with a long clock pulse
Solution: Repeated toggling can occur when J=K=1 and the clock pulse is too long.

Q52. Race-around can be eliminated using:

A) Master-slave JK flip-flop

B) OR gate

C) Decoder

D) Encoder

Answer: A) Master-slave JK flip-flop
Solution: Master-slave operation prevents repeated toggling during one clock pulse.

Q53. Setup time is the minimum time for which data must remain stable:

A) After clock edge

B) Before clock edge

C) After reset

D) Before power-off

Answer: B) Before clock edge
Solution: Data must be stable before the active clock edge.

Q54. Hold time is the minimum time data must remain stable:

A) Before clock edge

B) After clock edge

C) Before power-on

D) Before reset

Answer: B) After clock edge
Solution: Data must remain stable after the active edge.

Q55. Positive-edge triggering occurs during:

A) $1 \rightarrow 0$

B) $0 \rightarrow 1$

C) $1 \rightarrow 1$

D) $0 \rightarrow 0$

Answer: B) $0 \rightarrow 1$
Solution: A positive edge is a rising transition.

Registers

Q56. SISO means:

A) Serial In Serial Out

B) Serial In Parallel Out

C) Parallel In Serial Out

D) Parallel In Parallel Out

Answer: A) Serial In Serial Out
Solution: SISO shifts serial data in and out.

Q57. SIPO is used to convert:

A) Parallel data to serial

B) Serial data to parallel

C) Analog to digital

D) Digital to analog

Answer: B) Serial data to parallel
Solution: SIPO converts serial input into parallel output.

Q58. PISO converts:

A) Serial to parallel

B) Parallel to serial

C) Analog to digital

D) Digital to analog

Answer: B) Parallel to serial
Solution: PISO loads parallel data and shifts it out serially.

Q59. A 16-bit register requires:

A) 4 flip-flops

B) 8 flip-flops

C) 16 flip-flops

D) 32 flip-flops

Answer: C) 16 flip-flops
Solution: One flip-flop stores one bit.

Q60. A universal shift register can perform:

A) Only left shift

B) Only right shift

C) Left shift, right shift and parallel loading

D) Only counting

Answer: C) Left shift, right shift and parallel loading
Solution: Universal shift registers support multiple modes.

Counters

Q61. An asynchronous counter is also called:

A) Synchronous counter

B) Ripple counter

C) Ring counter

D) Johnson counter

Answer: B) Ripple counter
Solution: Clock transitions ripple through the flip-flops.

Q62. A 4-bit binary counter has:

A) 4 states

B) 8 states

C) 16 states

D) 32 states

Answer: C) 16 states
Solution: 2■ = 16 states.

Q63. A MOD-10 counter is called:

A) Ring counter

B) Decade counter

C) Johnson counter

D) MOD-16 counter

Answer: B) Decade counter
Solution: A decade counter has 10 states.

Q64. Minimum number of flip-flops required for a MOD-13 counter is:

A) 3

B) 4

C) 5

D) 13

Answer: B) 4
Solution: 2^3=8 is insufficient; 2■=16 is sufficient.

Q65. A 3-bit binary counter divides the input frequency at its MSB by:

A) 2

B) 4

C) 8

D) 16

Answer: C) 8
Solution: Three divide-by-2 stages give divide-by-8.

Q66. In a synchronous counter:

A) Only first flip-flop gets clock

B) All flip-flops receive the clock simultaneously

C) No flip-flop receives clock

D) Clock is random

Answer: B) All flip-flops receive the clock simultaneously
Solution: All stages share the clock.

Q67. A MOD-6 counter requires minimum:

A) 2 flip-flops

B) 3 flip-flops

C) 4 flip-flops

D) 6 flip-flops

Answer: B) 3 flip-flops
Solution: $2^3=8$, so 3 flip-flops are needed.

Q68. A ring counter with 5 flip-flops normally has:

A) 5 states

B) 10 states

C) 16 states

D) 32 states

Answer: A) 5 states
Solution: A ring counter normally has n states.

Q69. A 5-bit Johnson counter has:

A) 5 states

B) 10 states

C) 16 states

D) 32 states

Answer: B) 10 states
Solution: A Johnson counter has 2n states.

Q70. The major disadvantage of a ripple counter is:

A) No counting

B) Propagation delay

C) No clock

D) No output

Answer: B) Propagation delay
Solution: Ripple propagation creates cumulative delay.

Counter Design

Q71. A MOD-7 counter requires at least:

A) 2 flip-flops

B) 3 flip-flops

C) 4 flip-flops

D) 7 flip-flops

Answer: B) 3 flip-flops
Solution: $2^3=8$, enough for 7 states.

Q72. A MOD-17 counter requires at least:

A) 4 flip-flops

B) 5 flip-flops

C) 6 flip-flops

D) 17 flip-flops

Answer: B) 5 flip-flops
Solution: 2■=16 is insufficient; 2■=32 is sufficient.

Q73. The number of states in an n-bit binary counter is:

A) n

B) 2n

C) 2■

D) n^2

Answer: C) 2■
Solution: An n-bit counter has 2■ states.

Q74. A counter that counts 0,1,2,3,4,5 and then returns to 0 is:

A) MOD-5

B) MOD-6

C) MOD-7

D) MOD-8

Answer: B) MOD-6
Solution: There are six distinct states.

Q75. Counter state design generally begins with:

A) State diagram/table

B) Power calculation

C) Memory decoding

D) ADC conversion

Answer: A) State diagram/table
Solution: State design starts from the desired state sequence.

Memory

Q76. Which memory is volatile?

A) ROM

B) PROM

C) RAM

D) EEPROM

Answer: C) RAM
Solution: RAM normally loses data when power is removed.

Q77. Which memory requires periodic refreshing?

A) SRAM

B) DRAM

C) ROM

D) EEPROM

Answer: B) DRAM
Solution: DRAM stores charge that must be refreshed.

Q78. SRAM generally uses:

A) Capacitor-only cells

B) Flip-flop-based cells

C) Magnetic cells

D) Optical cells

Answer: B) Flip-flop-based cells
Solution: SRAM cells are typically bistable/flip-flop based.

Q79. EPROM is erased using:

A) Electrical pulses

B) Ultraviolet light

C) Magnetic field

D) Heat only

Answer: B) Ultraviolet light
Solution: Traditional EPROM uses UV light.

Q80. EEPROM can be erased:

A) Electrically

B) Only using UV light

C) Mechanically

D) Magnetically

Answer: A) Electrically
Solution: EEPROM is electrically erasable.

Memory Organization & PLD

Q81. A memory with 12 address lines can address:

A) 1024 locations

B) 2048 locations

C) 4096 locations

D) 8192 locations

Answer: C) 4096 locations
Solution: $2^{12} = 4096$.

Q82. A 1K × 8 memory contains:

A) 1024 words of 8 bits

B) 1000 words of 8 bits

C) 1024 words of 16 bits

D) 2048 words of 8 bits

Answer: A) 1024 words of 8 bits
Solution: 1K means 1024 words; each word is 8 bits.

Q83. PLA has:

A) Programmable AND and OR arrays

B) Fixed AND and OR arrays

C) Programmable OR only

D) Programmable AND only

Answer: A) Programmable AND and OR arrays
Solution: Both planes are programmable in a PLA.

Q84. PAL generally has:

A) Programmable AND and fixed OR

B) Fixed AND and programmable OR

C) Both fixed

D) Both absent

Answer: A) Programmable AND and fixed OR
Solution: A standard PAL has programmable AND and fixed OR.

Q85. FPGA stands for:

A) Field Programmable Gate Array

B) Fast Programmable Gate Array

C) Field Processing Gate Array

D) Fixed Programmable Gate Array

Answer: A) Field Programmable Gate Array
Solution: FPGA means Field Programmable Gate Array.

Logic Families

Q86. TTL stands for:

A) Transistor-Transistor Logic

B) Transistor Transfer Logic

C) Total Transistor Logic

D) Two Transistor Logic

Answer: A) Transistor-Transistor Logic
Solution: TTL is a transistor-transistor logic family.

Q87. CMOS is known for:

A) High static power consumption

B) Low static power consumption

C) Very low input impedance

D) No noise immunity

Answer: B) Low static power consumption
Solution: CMOS has very low static power consumption.

Q88. Fan-out represents:

A) Number of inputs of a gate

B) Number of loads a gate output can drive

C) Propagation delay

D) Power supply voltage

Answer: B) Number of loads a gate output can drive
Solution: Fan-out is the load-driving capability of an output.

Q89. Propagation delay is the time between:

A) Input transition and output response

B) Two power supplies

C) Two memory locations

D) Two input pins

Answer: A) Input transition and output response
Solution: It is the delay from an input change to the corresponding output change.

Q90. Noise margin indicates:

A) Maximum clock frequency

B) Tolerance against unwanted noise

C) Number of inputs

D) Memory capacity

Answer: B) Tolerance against unwanted noise
Solution: Noise margin measures immunity to noise.

ADC, DAC & Error Detection

Q91. ADC stands for:

A) Analog-to-Digital Converter

B) Automatic Digital Counter

C) Analog Data Controller

D) Advanced Digital Circuit

Answer: A) Analog-to-Digital Converter
Solution: ADC converts analog quantities to digital codes.

Q92. An 8-bit ADC has:

A) 128 levels

B) 256 levels

C) 512 levels

D) 1024 levels

Answer: B) 256 levels
Solution: 2■ = 256 levels.

Q93. DAC performs:

A) Analog-to-digital conversion

B) Digital-to-analog conversion

C) Digital-to-digital conversion

D) Analog-to-analog conversion

Answer: B) Digital-to-analog conversion
Solution: DAC converts digital code to an analog output.

Q94. Quantization error is associated with:

A) ADC

B) Counter

C) Register

D) Decoder

Answer: A) ADC
Solution: Quantization occurs during analog-to-digital conversion.

Q95. A sample-and-hold circuit is commonly used in:

A) ADC systems

B) Counters

C) Registers only

D) Decoders

Answer: A) ADC systems
Solution: It holds the analog input steady during conversion.

Q96. Which gate is commonly used to generate parity?

A) AND

B) OR

C) XOR

D) NAND

Answer: C) XOR
Solution: XOR is widely used in parity generation.

Q97. In even parity, the total number of 1s including the parity bit must be:

A) Odd

B) Even

C) Zero

D) One

Answer: B) Even
Solution: Even parity requires an even total number of 1s.

Q98. Hamming code is primarily used for:

A) Data compression

B) Error detection and correction

C) Multiplexing

D) Frequency division

Answer: B) Error detection and correction
Solution: Hamming code can detect and correct certain bit errors.

Q99. Which combination represents a sequential circuit?

A) AND gate

B) Decoder

C) Flip-flop

D) Multiplexer

Answer: C) Flip-flop
Solution: A flip-flop stores state, making it sequential.

Q100. A digital circuit uses 5 input variables. The maximum number of different input combinations is:

A) 10

B) 16

C) 25

D) 32

Answer: D) 32
Solution: Number of combinations = 2■ = 32.