ECE 213 – Digital Electronics

100 More Hard MCQs — Set 2

Advanced, numerical, design-based and tricky concept-wise practice

Boolean Algebra & K-Map

Q1. Simplify: F = AB + A'C + BC

A) AB + A'C

B) AB + BC

C) A'C + BC

D) AB + A'C + BC

Answer: A) AB + A'C
Solution: By the consensus theorem, BC is redundant. Therefore F = AB + A'C.

Q2. The dual of A + 0 = A is:

A) A · 0 = A

B) A · 1 = A

C) A + 1 = A

D) A' + 0 = A

Answer: B) A · 1 = A
Solution: The dual is obtained by interchanging + with · and 0 with 1.

Q3. Which expression represents the complement of A + BC?

A) A' + B'C'

B) A'(B' + C')

C) A'B'C'

D) A' + B'C'

Answer: B) A'(B' + C')
Solution: Apply De Morgan's theorem: (A + BC)' = A'(BC)' = A'(B' + C').

Q4. A 5-variable K-map contains:

A) 16 cells

B) 25 cells

C) 32 cells

D) 64 cells

Answer: C) 32 cells
Solution: Number of cells = 2^5 = 32.

Q5. In a 5-variable K-map, a group of 8 cells leaves:

A) 1 variable

B) 2 variables

C) 3 variables

D) 4 variables

Answer: B) 2 variables
Solution: A group of 8 out of 32 cells eliminates 3 variables and leaves 2 variables.

Q6. The maximum possible group in a 4-variable K-map containing all cells contains:

A) 4

B) 8

C) 12

D) 16

Answer: D) 16
Solution: A 4-variable K-map has 16 cells.

Q7. If F(A,B,C,D) = Σ(0,2,8,10), the simplified expression is:

A) B'D'

B) B'D

C) BD'

D) BC'

Answer: A) B'D'
Solution: All listed minterms have B=0 and D=0; A and C vary. Hence F=B'D'.

Q8. If all minterms of a Boolean function are included, the function simplifies to:

A) 0

B) 1

C) A

D) A'

Answer: B) 1
Solution: The sum of all possible minterms covers every input combination, so F=1.

Q9. Which condition is most useful for obtaining the largest K-map group?

A) Avoid adjacent cells

B) Use don't-care cells when beneficial

C) Group only corner cells

D) Group diagonal cells

Answer: B) Use don't-care cells when beneficial
Solution: Don't-care cells can be treated as 0 or 1 to form larger groups.

Q10. In POS K-map minimization, groups are formed using:

A) 1s

B) 0s

C) Both equally

D) Complements only

Answer: B) 0s
Solution: POS minimization groups zero cells.

Advanced Combinational Circuits

Q11. A full adder can be represented by the Sum equation:

A) A+B+Cin

B) A XOR B XOR Cin

C) ABCin

D) AB + Cin

Answer: B) A XOR B XOR Cin
Solution: The full-adder sum is A XOR B XOR Cin.

Q12. The carry output of a full adder is:

A) AB + ACin + BCin

B) A+B+Cin

C) A XOR B XOR Cin

D) ABCin

Answer: A) AB + ACin + BCin
Solution: Carry is 1 when at least two inputs are 1.

Q13. A 4-bit parallel adder using ripple carry has the main limitation of:

A) Low fan-in

B) Carry propagation delay

C) No carry output

D) No sum output

Answer: B) Carry propagation delay
Solution: Carry must propagate from one stage to the next.

Q14. Carry Look-Ahead logic reduces:

A) Number of input bits

B) Carry propagation delay

C) Number of outputs

D) Memory size

Answer: B) Carry propagation delay
Solution: Carry signals are computed more quickly in parallel.

Q15. In a full subtractor, the three inputs are:

A) A, B, Sum

B) A, B, Borrow-in

C) A, Difference, Borrow

D) A, Carry, Borrow

Answer: B) A, B, Borrow-in
Solution: The inputs are minuend, subtrahend and borrow-in.

Q16. A 4-bit magnitude comparator provides:

A) 2 outputs

B) 3 outputs

C) 4 outputs

D) 8 outputs

Answer: B) 3 outputs
Solution: It indicates A>B, A=B and A<B.

Q17. For two equal binary numbers, a magnitude comparator activates:

A) A>B

B) A<B

C) A=B

D) All three

Answer: C) A=B
Solution: Equal inputs activate the equality output.

Q18. Which circuit can be used to perform binary addition and subtraction using the same hardware?

A) MUX

B) Decoder

C) Adder-subtractor

D) Encoder

Answer: C) Adder-subtractor
Solution: An adder-subtractor uses controlled complementation of the second operand.

Q19. In a 2's-complement adder-subtractor, subtraction is performed by:

A) Adding the complement of B plus 1

B) Subtracting A from B directly

C) Multiplying B by 2

D) Removing the carry

Answer: A) Adding the complement of B plus 1
Solution: A-B = A + (2's complement of B).

Q20. Overflow in signed 2's-complement addition occurs when:

A) Positive + positive gives negative

B) Negative + negative gives positive

C) Either A or B is zero

D) Both A and B are different signs

Answer: A) Positive + positive gives negative
Solution: Positive-plus-positive overflow gives a negative result; negative-plus-negative overflow gives a positive result.

Advanced MUX / DEMUX

Q21. A 32-to-1 MUX requires:

A) 4 select lines

B) 5 select lines

C) 6 select lines

D) 8 select lines

Answer: B) 5 select lines
Solution: 2^5=32, so 5 select lines are required.

Q22. How many 2-to-1 MUXes are required to construct one 8-to-1 MUX?

A) 4

B) 6

C) 7

D) 8

Answer: C) 7
Solution: A binary MUX tree requires 8-1 = 7 two-to-one MUXes.

Q23. A 16-to-1 MUX can be constructed using:

A) Five 4-to-1 MUXes

B) Four 4-to-1 MUXes

C) Two 8-to-1 MUXes only

D) Sixteen 2-to-1 MUXes only

Answer: A) Five 4-to-1 MUXes
Solution: Four first-stage 4:1 MUXes plus one final 4:1 MUX = 5.

Q24. A 4-to-1 MUX can implement a Boolean function of:

A) Only 2 variables

B) Up to 4 variables depending on implementation

C) Only 4 variables

D) No Boolean function

Answer: B) Up to 4 variables depending on implementation
Solution: Select lines and data inputs can be assigned to implement functions with additional variables.

Q25. If select lines of a 4-to-1 MUX are S1S0=10, selected input is:

A) I0

B) I1

C) I2

D) I3

Answer: C) I2
Solution: Binary 10 corresponds to decimal 2, selecting I2.

Q26. In a DEMUX, select lines determine:

A) Input value

B) Which output receives the input

C) Clock frequency

D) Memory size

Answer: B) Which output receives the input
Solution: Select lines route the input to one output.

Q27. A decoder with 4 input lines can have a maximum of:

A) 4 outputs

B) 8 outputs

C) 16 outputs

D) 32 outputs

Answer: C) 16 outputs
Solution: 2^4=16 outputs.

Q28. An active-low decoder output is selected when the output becomes:

A) 1

B) 0

C) X

D) Z

Answer: B) 0
Solution: Active-low signals are asserted at logic 0.

Q29. A BCD-to-7-segment decoder requires:

A) 2 inputs

B) 3 inputs

C) 4 inputs

D) 7 inputs

Answer: C) 4 inputs
Solution: BCD uses four input bits.

Q30. Priority encoding solves the problem of:

A) No input

B) Multiple simultaneous active inputs

C) Clock delay

D) Memory refresh

Answer: B) Multiple simultaneous active inputs
Solution: It assigns priority when multiple inputs are active.

Flip-Flop Advanced

Q31. The characteristic equation of a JK flip-flop is:

A) Q(next)=J+K

B) Q(next)=JQ + KQ'

C) Q(next)=JQ' + K'Q

D) Q(next)=JK

Answer: C) Q(next)=JQ' + K'Q
Solution: The standard JK characteristic equation is Q(next)=JQ' + K'Q.

Q32. The characteristic equation of a D flip-flop is:

A) Q(next)=D

B) Q(next)=D'

C) Q(next)=Q

D) Q(next)=D+Q

Answer: A) Q(next)=D
Solution: The next state follows D.

Q33. The characteristic equation of a T flip-flop is:

A) Q(next)=T

B) Q(next)=TQ

C) Q(next)=T XOR Q

D) Q(next)=T'Q

Answer: C) Q(next)=T XOR Q
Solution: T=1 toggles Q and T=0 holds Q.

Q34. To make a JK flip-flop behave as a T flip-flop:

A) J=0,K=0

B) J=K=T

C) J=T,K=0

D) J=1,K=T

Answer: B) J=K=T
Solution: Connecting J and K together to T gives T-FF behavior.

Q35. To make a JK flip-flop behave as a D flip-flop:

A) J=D, K=D'

B) J=D', K=D

C) J=K=D

D) J=0,K=D

Answer: A) J=D, K=D'
Solution: J=D and K=D' produces D-FF behavior.

Q36. To make a D flip-flop behave like a T flip-flop:

A) D=T

B) D=T'

C) D=T XOR Q

D) D=Q

Answer: C) D=T XOR Q
Solution: D must equal the desired next state, T XOR Q.

Q37. The excitation table is primarily used for:

A) Finding required inputs for a desired state transition

B) Measuring voltage

C) Measuring frequency

D) Memory addressing

Answer: A) Finding required inputs for a desired state transition
Solution: It maps present/next states to required FF inputs.

Q38. For a JK flip-flop, transition 0 → 1 requires:

A) J=0,K=0

B) J=0,K=1

C) J=1,K=X

D) J=X,K=1

Answer: C) J=1,K=X
Solution: J must be 1; K is don't-care.

Q39. For a JK flip-flop, transition 1 → 0 requires:

A) J=0,K=X

B) J=1,K=X

C) J=X,K=0

D) J=X,K=1

Answer: D) J=X,K=1
Solution: K must be 1; J is don't-care.

Q40. A master-slave flip-flop uses:

A) Two latches

B) Two counters

C) Two decoders

D) Two MUXes

Answer: A) Two latches
Solution: A master and slave latch operate on opposite clock phases.

Timing & Sequential Logic

Q41. If propagation delay of each flip-flop in a 4-bit ripple counter is 20 ns, approximate worst-case ripple delay is:

A) 20 ns

B) 40 ns

C) 80 ns

D) 100 ns

Answer: C) 80 ns
Solution: Worst-case cumulative delay is approximately 4×20 ns = 80 ns.

Q42. Setup-time violation may result in:

A) Metastability

B) Higher memory capacity

C) Frequency multiplication

D) Decoding

Answer: A) Metastability
Solution: Violating setup time can cause metastability.

Q43. Hold-time violation occurs when data changes:

A) Too early before clock

B) Too soon after clock edge

C) Before power-up

D) During reset only

Answer: B) Too soon after clock edge
Solution: Data must remain stable for the specified hold interval after the edge.

Q44. Clock skew means:

A) Difference in arrival time of clock signals

B) Difference in data values

C) Memory failure

D) Output inversion

Answer: A) Difference in arrival time of clock signals
Solution: Clock skew is the timing difference between clock arrivals.

Q45. A flip-flop with asynchronous clear can be cleared:

A) Only on the clock edge

B) Independently of the clock

C) Only during positive edge

D) Only during negative edge

Answer: B) Independently of the clock
Solution: Asynchronous controls operate independently of the clock.

Registers

Q46. A 4-bit SIPO register requires at least:

A) 2 flip-flops

B) 4 flip-flops

C) 8 flip-flops

D) 16 flip-flops

Answer: B) 4 flip-flops
Solution: One flip-flop is needed per stored bit.

Q47. In a right-shift register, bits generally move toward:

A) MSB

B) LSB

C) Both simultaneously

D) Neither

Answer: B) LSB
Solution: A right shift moves bits toward the least significant position.

Q48. A bidirectional shift register can:

A) Only shift left

B) Only shift right

C) Shift both left and right

D) Only parallel load

Answer: C) Shift both left and right
Solution: Direction can be selected.

Q49. A universal shift register normally supports:

A) Serial shifting and parallel loading

B) Only counting

C) Only decoding

D) Only inversion

Answer: A) Serial shifting and parallel loading
Solution: Universal shift registers support serial and parallel modes.

Q50. The primary storage element in a shift register is:

A) AND gate

B) Flip-flop

C) Decoder

D) MUX only

Answer: B) Flip-flop
Solution: Each flip-flop stores one bit.

Advanced Counters

Q51. A 4-bit ripple counter is clocked at 16 MHz. Its MSB frequency is:

A) 8 MHz

B) 4 MHz

C) 2 MHz

D) 1 MHz

Answer: D) 1 MHz
Solution: Four divide-by-2 stages give 16 MHz/16 = 1 MHz.

Q52. A MOD-12 counter requires minimum:

A) 3 flip-flops

B) 4 flip-flops

C) 5 flip-flops

D) 12 flip-flops

Answer: B) 4 flip-flops
Solution: 2^3=8 is insufficient; 2^4=16 is sufficient.

Q53. A MOD-31 counter requires:

A) 4 flip-flops

B) 5 flip-flops

C) 6 flip-flops

D) 31 flip-flops

Answer: B) 5 flip-flops
Solution: 2^5=32 states, enough for 31.

Q54. A MOD-32 counter requires:

A) 4 flip-flops

B) 5 flip-flops

C) 6 flip-flops

D) 8 flip-flops

Answer: B) 5 flip-flops
Solution: 2^5=32.

Q55. A 6-bit binary counter has how many states?

A) 32

B) 64

C) 128

D) 256

Answer: B) 64
Solution: 2^6=64.

Q56. A decade counter has how many unused states when implemented using four flip-flops?

A) 4

B) 5

C) 6

D) 10

Answer: C) 6
Solution: Four FFs provide 16 states; 16–10=6 unused.

Q57. A 4-bit ring counter normally requires initialization to:

A) All 0s

B) One-hot state

C) All 1s only

D) Random state

Answer: B) One-hot state
Solution: A standard ring counter begins with one active bit.

Q58. A Johnson counter with n flip-flops has:

A) n states

B) 2n states

C) 2^n states

D) n^2 states

Answer: B) 2n states
Solution: A Johnson counter has 2n valid states.

Q59. A 4-bit Johnson counter has:

A) 4 states

B) 8 states

C) 16 states

D) 32 states

Answer: B) 8 states
Solution: 2×4=8.

Q60. Compared with ripple counters, synchronous counters generally have:

A) Greater cumulative propagation delay

B) Lower timing uncertainty

C) No clock

D) No flip-flops

Answer: B) Lower timing uncertainty
Solution: All flip-flops are clocked together, reducing ripple delay.

Counter Design & State Machines

Q61. A MOD-5 counter has how many unused states if built using 3 flip-flops?

A) 1

B) 2

C) 3

D) 4

Answer: C) 3
Solution: Three FFs give 8 states; 8–5=3 unused states.

Q62. A state machine with 8 states requires minimum:

A) 2 state bits

B) 3 state bits

C) 4 state bits

D) 8 state bits

Answer: B) 3 state bits
Solution: 2^3=8.

Q63. A Moore machine output depends on:

A) Input only

B) Present state only

C) Next state only

D) Clock frequency only

Answer: B) Present state only
Solution: Moore outputs depend on state.

Q64. A Mealy machine output depends on:

A) Present state and input

B) State only

C) Input only

D) Clock only

Answer: A) Present state and input
Solution: Mealy output is a function of state and input.

Q65. Compared with a Moore machine, a Mealy machine can generally respond to input changes:

A) Only after two clocks

B) More quickly

C) Never

D) Only after reset

Answer: B) More quickly
Solution: Mealy outputs can change directly with input changes.

Memory

Q66. A memory has 14 address lines and 8-bit words. Its capacity is:

A) 8 KB

B) 16 KB

C) 32 KB

D) 64 KB

Answer: B) 16 KB
Solution: 2^14×8 bits = 16,384 bytes = 16 KB.

Q67. A 64K × 16 memory has total storage capacity:

A) 64 KB

B) 128 KB

C) 256 KB

D) 512 KB

Answer: B) 128 KB
Solution: 64K words × 16 bits = 128 KB.

Q68. Which memory is generally faster?

A) DRAM

B) SRAM

C) Magnetic disk

D) Optical disk

Answer: B) SRAM
Solution: SRAM is typically faster than DRAM.

Q69. The main reason DRAM requires refresh is:

A) Gate leakage only

B) Charge leakage from storage capacitors

C) Clock skew

D) Address decoding

Answer: B) Charge leakage from storage capacitors
Solution: DRAM cells store information as capacitor charge.

Q70. Flash memory is a type of:

A) SRAM

B) EEPROM

C) DRAM

D) PROM only

Answer: B) EEPROM
Solution: Flash is a nonvolatile EEPROM technology.

Memory Expansion

Q71. To construct a 4K × 8 memory using 1K × 8 chips, how many chips are required?

A) 2

B) 4

C) 8

D) 16

Answer: B) 4
Solution: Four 1K×8 chips provide 4K×8.

Q72. To construct a 1K × 16 memory using 1K × 4 chips, required chips are:

A) 2

B) 4

C) 8

D) 16

Answer: B) 4
Solution: Four 1K×4 chips in parallel provide 1K×16.

Q73. Address decoding is primarily used for:

A) Selecting memory chips

B) Increasing clock frequency

C) Generating analog signals

D) Reducing word size

Answer: A) Selecting memory chips
Solution: Address decoding selects the required memory device/location.

Q74. A 2K memory requires how many address lines?

A) 8

B) 10

C) 11

D) 12

Answer: C) 11
Solution: 2K=2048=2^11.

Q75. A 32K × 8 memory has how many data lines?

A) 5

B) 8

C) 16

D) 32

Answer: B) 8
Solution: The word width is 8 bits.

PLD & Logic Families

Q76. Which PLD is generally more flexible?

A) PAL

B) PLA

C) Fixed ROM

D) Decoder

Answer: B) PLA
Solution: Both AND and OR arrays are programmable in a PLA.

Q77. CPLD stands for:

A) Complex Programmable Logic Device

B) Central Programmable Logic Device

C) Computer Programmable Logic Decoder

D) Complex Parallel Logic Decoder

Answer: A) Complex Programmable Logic Device
Solution: CPLD means Complex Programmable Logic Device.

Q78. FPGA logic is generally based on:

A) Configurable logic blocks

B) Fixed AND gates only

C) Transformers

D) Analog amplifiers

Answer: A) Configurable logic blocks
Solution: FPGAs use configurable logic blocks and routing.

Q79. CMOS logic has high:

A) Static power consumption

B) Input impedance

C) Output delay only

D) Leakage current always

Answer: B) Input impedance
Solution: MOS inputs have very high impedance.

Q80. Fan-in refers to:

A) Number of loads

B) Number of inputs to a gate

C) Power consumption

D) Clock frequency

Answer: B) Number of inputs to a gate
Solution: Fan-in is the number of inputs a gate accepts.

Timing, Noise & Performance

Q81. If a logic gate has a propagation delay of 10 ns, its approximate maximum theoretical toggle frequency based solely on one delay is:

A) 10 MHz

B) 25 MHz

C) 50 MHz

D) 100 MHz

Answer: D) 100 MHz
Solution: Using 1/10 ns gives 100 MHz as a simple one-delay reciprocal estimate; real maximum operating frequency depends on the complete timing path.

Q82. Increasing fan-out generally causes:

A) No loading effect

B) Increased loading

C) Zero propagation delay

D) Lower memory capacity

Answer: B) Increased loading
Solution: More loads increase capacitive loading.

Q83. Noise margin is improved when:

A) Logic levels have better separation

B) Supply is always zero

C) Fan-out is infinite

D) Delay is infinite

Answer: A) Logic levels have better separation
Solution: Greater separation between valid logic levels improves noise tolerance.

Q84. Power-delay product is a measure of:

A) Speed-power tradeoff

B) Memory size

C) Number of inputs

D) Number of states

Answer: A) Speed-power tradeoff
Solution: PDP combines power consumption and propagation delay.

Q85. CMOS dynamic power consumption is strongly related to:

A) Switching activity and frequency

B) Memory address only

C) Number of minterms

D) K-map size

Answer: A) Switching activity and frequency
Solution: Dynamic power increases with switching activity and frequency.

ADC / DAC

Q86. An ideal 10-bit ADC provides:

A) 256 levels

B) 512 levels

C) 1024 levels

D) 2048 levels

Answer: C) 1024 levels
Solution: 2^10=1024 levels.

Q87. Compared with an 8-bit ADC, a 10-bit ADC has:

A) Lower resolution

B) Higher resolution

C) Same resolution

D) No quantization

Answer: B) Higher resolution
Solution: More bits give finer quantization.

Q88. An ideal N-bit ADC has:

A) N levels

B) 2N levels

C) 2^N levels

D) N^2 levels

Answer: C) 2^N levels
Solution: An N-bit code provides 2^N possible levels.

Q89. Increasing ADC resolution generally:

A) Reduces quantization step size

B) Increases quantization step size

C) Removes sampling

D) Eliminates all errors

Answer: A) Reduces quantization step size
Solution: More levels divide the range into smaller steps.

Q90. A DAC converts:

A) Analog signal to digital code

B) Digital code to analog signal

C) Digital to digital

D) Analog to analog

Answer: B) Digital code to analog signal
Solution: DAC produces an analog output from a digital code.

Error Detection & Advanced Mixed

Q91. A parity bit can reliably detect:

A) Every possible multi-bit error

B) Any odd number of bit errors

C) Only one specific bit error

D) No errors

Answer: B) Any odd number of bit errors
Solution: Parity changes for any odd number of bit flips.

Q92. For even parity, data 1011001 requires parity bit:

A) 0

B) 1

C) X

D) Cannot determine

Answer: A) 0
Solution: There are four 1s, already even, so parity bit is 0.

Q93. Hamming distance between 10101 and 10011 is:

A) 1

B) 2

C) 3

D) 4

Answer: B) 2
Solution: They differ in two bit positions.

Q94. A code with minimum Hamming distance 3 can:

A) Detect 1 error only

B) Correct 1-bit error

C) Correct 2-bit errors always

D) Detect no errors

Answer: B) Correct 1-bit error
Solution: d_min=3 permits correction of floor((3–1)/2)=1 error.

Q95. XOR of three inputs is 1 when the number of 1s is:

A) Even

B) Odd

C) Zero only

D) Three only

Answer: B) Odd
Solution: XOR is 1 for odd parity.

Q96. If A XOR B = 0, then:

A) A and B must be different

B) A and B must be equal

C) A=1 only

D) B=1 only

Answer: B) A and B must be equal
Solution: XOR is zero when inputs are equal.

Q97. A NAND gate output becomes 0 only when:

A) All inputs are 0

B) At least one input is 0

C) All inputs are 1

D) Inputs are different

Answer: C) All inputs are 1
Solution: NAND is the complement of AND.

Q98. A NOR gate can be used as an inverter by:

A) Connecting inputs together

B) Removing all inputs

C) Adding a flip-flop

D) Connecting to a decoder

Answer: A) Connecting inputs together
Solution: With tied inputs, NOR gives (A+A)'=A'.

Q99. Which circuit is fundamentally memoryless?

A) Counter

B) Register

C) Decoder

D) Flip-flop

Answer: C) Decoder
Solution: A decoder is combinational and has no stored state.

Q100. A circuit has 4 flip-flops. The maximum number of distinct states it can represent is:

A) 4

B) 8

C) 16

D) 32

Answer: C) 16
Solution: 2^4=16 states.