ECE 213 – Digital Electronics

500 MCQs with Answers & Short Explanations

LPU-oriented practice set covering the major Digital Electronics topics

UNIT 1: Number Systems & Codes

Q1. The radix of binary number system is

A) 2

B) 8

C) 10

D) 16

Answer: A) 2
Explanation: Binary uses 0 and 1.

Q2. The radix of hexadecimal number system is

A) 2

B) 8

C) 10

D) 16

Answer: D) 16
Explanation: Hexadecimal has 16 symbols.

Q3. Decimal equivalent of (1010)■ is

A) 8

B) 10

C) 12

D) 14

Answer: B) 10
Explanation: 8 + 2 = 10.

Q4. Decimal equivalent of (1111)■ is

A) 12

B) 13

C) 14

D) 15

Answer: D) 15
Explanation: 8+4+2+1 = 15.

Q5. Binary equivalent of decimal 5 is

A) 100

B) 101

C) 110

D) 111

Answer: B) 101
Explanation: 5 = 4+1.

Q6. Binary equivalent of decimal 12 is

A) 1010

B) 1011

C) 1100

D) 1110

Answer: C) 1100
Explanation: 12 = 8+4.

Q7. Octal number system has how many symbols?

A) 2

B) 8

C) 10

D) 16

Answer: B) 8
Explanation: Digits are 0–7.

Q8. Which digits are used in octal system?

A) 0–7

B) 0–8

C) 1–8

D) 0–9

Answer: A) 0–7
Explanation: Octal uses 0 through 7.

Q9. Hexadecimal equivalent of decimal 15 is

A) E

B) F

C) A

D) D

Answer: B) F
Explanation: 15 is F in hexadecimal.

Q10. Hexadecimal equivalent of decimal 10 is

A) A

B) B

C) C

D) D

Answer: A) A
Explanation: 10 is A in hexadecimal.

Q11. The binary equivalent of hexadecimal A is

A) 1000

B) 1001

C) 1010

D) 1110

Answer: C) 1010
Explanation: A■■ = 1010■.

Q12. One hexadecimal digit represents how many bits?

A) 2

B) 3

C) 4

D) 8

Answer: C) 4
Explanation: Each hex digit maps to 4 bits.

Q13. One octal digit represents how many bits?

A) 2

B) 3

C) 4

D) 8

Answer: B) 3
Explanation: Each octal digit maps to 3 bits.

Q14. BCD stands for

A) Binary Coded Decimal

B) Binary Converted Digit

C) Bit Coded Decimal

D) Binary Code Data

Answer: A) Binary Coded Decimal
Explanation: BCD represents each decimal digit with four bits.

Q15. In Gray code, consecutive values differ by

A) One bit

B) Two bits

C) Three bits

D) Four bits

Answer: A) One bit
Explanation: Gray code is unit-distance.

Q16. 1's complement of 101100 is

A) 010011

B) 010100

C) 101011

D) 110011

Answer: A) 010011
Explanation: Invert each bit.

Q17. 2's complement is obtained by

A) Adding 1 directly

B) 1's complement plus 1

C) Subtracting 1

D) Multiplying by 2

Answer: B) 1's complement plus 1
Explanation: That is the standard procedure.

Q18. Four bits are called

A) Byte

B) Nibble

C) Word

D) Register

Answer: B) Nibble
Explanation: A nibble contains four bits.

Q19. Eight bits are called

A) Nibble

B) Byte

C) Word

D) Digit

Answer: B) Byte
Explanation: A byte contains eight bits.

Q20. The most significant bit is abbreviated as

A) LSB

B) MSB

C) MSS

D) MBS

Answer: B) MSB
Explanation: MSB means most significant bit.

Q21. An AND gate outputs 1 when

A) Any input is 1

B) All inputs are 1

C) All inputs are 0

D) Inputs differ

Answer: B) All inputs are 1
Explanation: AND requires every input to be 1.

Q22. An OR gate outputs 0 when

A) All inputs are 0

B) Any input is 1

C) All inputs are 1

D) Inputs differ

Answer: A) All inputs are 0
Explanation: OR is 0 only when all inputs are 0.

Q23. A NOT gate is also called

A) Inverter

B) Buffer

C) Adder

D) Decoder

Answer: A) Inverter
Explanation: It complements the input.

Q24. NAND is equivalent to

A) AND followed by NOT

B) OR followed by NOT

C) NOT followed by OR

D) XOR followed by NOT

Answer: A) AND followed by NOT
Explanation: NAND = NOT(AND).

Q25. NOR is equivalent to

A) AND followed by NOT

B) OR followed by NOT

C) XOR followed by NOT

D) NOT only

Answer: B) OR followed by NOT
Explanation: NOR = NOT(OR).

Q26. NAND and NOR are called

A) Basic gates

B) Universal gates

C) Memory gates

D) Sequential gates

Answer: B) Universal gates
Explanation: Either can implement any Boolean function.

Q27. XOR output is 1 when inputs are

A) Same

B) Different

C) Both 0

D) Both 1

Answer: B) Different
Explanation: XOR detects inequality.

Q28. XNOR output is 1 when inputs are

A) Different

B) Same

C) Both 0 only

D) Both 1 only

Answer: B) Same
Explanation: XNOR detects equality.

Q29. A + 0 equals

A) 0

B) A

C) 1

D) A'

Answer: B) A
Explanation: Identity law.

Q30. A · 1 equals

A) 0

B) A

C) 1

D) A'

Answer: B) A
Explanation: Identity law.

Q31. SOP stands for

A) Sum of Products

B) Series of Products

C) Sum of Powers

D) System of Products

Answer: A) Sum of Products
Explanation: SOP is Sum of Products.

Q32. POS stands for

A) Product of Sums

B) Power of Sums

C) Product of Signals

D) Parallel Output System

Answer: A) Product of Sums
Explanation: POS is Product of Sums.

Q33. A minterm is a

A) Product term

B) Sum term

C) Complement only

D) Constant only

Answer: A) Product term
Explanation: Minterms are product terms containing all variables.

Q34. A maxterm is a

A) Product term

B) Sum term

C) XOR term

D) NOT term

Answer: B) Sum term
Explanation: Maxterms are sum terms.

Q35. A 3-variable K-map has

A) 4 cells

B) 6 cells

C) 8 cells

D) 16 cells

Answer: C) 8 cells
Explanation: $2^3 = 8$.

Q36. A 4-variable K-map has

A) 4 cells

B) 8 cells

C) 16 cells

D) 32 cells

Answer: C) 16 cells
Explanation: 2■ = 16.

Q37. Valid K-map group sizes are

A) Any number

B) Powers of two

C) Odd only

D) Prime only

Answer: B) Powers of two
Explanation: Groups contain 1,2,4,8,... cells.

Q38. For SOP simplification, group

A) 0s

B) 1s

C) X only

D) All cells

Answer: B) 1s
Explanation: SOP groups 1s.

Q39. For POS simplification, group

A) 0s

B) 1s

C) X only

D) None

Answer: A) 0s
Explanation: POS groups 0s.

Q40. K-map cells use

A) Binary sequence

B) Gray-code sequence

C) Decimal sequence

D) Random sequence

Answer: B) Gray-code sequence
Explanation: Adjacent cells differ in one variable.

Q41. A half adder adds

A) Two bits

B) Three bits

C) Four bits

D) One byte

Answer: A) Two bits
Explanation: It has two inputs.

Q42. Half adder outputs are

A) Sum and Carry

B) Difference and Borrow

C) Product and Carry

D) Sum only

Answer: A) Sum and Carry
Explanation: Its outputs are S and C.

Q43. Half-adder Sum uses

A) AND

B) OR

C) XOR

D) NOR

Answer: C) XOR
Explanation: S = A XOR B.

Q44. Half-adder Carry uses

A) AND

B) OR

C) XOR

D) NOT

Answer: A) AND
Explanation: C = AB.

Q45. A full adder has inputs

A) 2

B) 3

C) 4

D) 5

Answer: B) 3
Explanation: A, B and carry-in.

Q46. Full-adder outputs are

A) Sum and Carry

B) Difference and Borrow

C) Product and Carry

D) Sum only

Answer: A) Sum and Carry
Explanation: It produces sum and carry-out.

Q47. A full adder can be built using

A) Two half adders and OR

B) One NOT

C) Two OR only

D) One decoder

Answer: A) Two half adders and OR
Explanation: Two half adders plus an OR gate.

Q48. A half subtractor has outputs

A) Sum and Carry

B) Difference and Borrow

C) Product and Carry

D) Difference only

Answer: B) Difference and Borrow
Explanation: It subtracts two bits.

Q49. A full subtractor has inputs

A) 2

B) 3

C) 4

D) 5

Answer: B) 3
Explanation: A, B and borrow-in.

Q50. Carry look-ahead adder is designed to

A) Reduce carry delay

B) Increase delay

C) Store data

D) Decode data

Answer: A) Reduce carry delay
Explanation: It speeds carry computation.

UNIT 2: Boolean Algebra & Logic Gates

Q51. MUX stands for

A) Multiplexer

B) Multiplier

C) Memory Unit

D) Modulator

Answer: A) Multiplexer
Explanation: A multiplexer selects data.

Q52. A multiplexer is also called

A) Data selector

B) Data distributor

C) Encoder

D) Counter

Answer: A) Data selector
Explanation: It selects one of many inputs.

Q53. A 4-to-1 MUX has

A) 4 inputs and 1 output

B) 1 input and 4 outputs

C) 4 and 4

D) 2 and 1

Answer: A) 4 inputs and 1 output
Explanation: Four data inputs, one output.

Q54. A 4-to-1 MUX needs

A) 1

B) 2

C) 3

D) 4

Answer: B) 2
Explanation: $2^2 = 4$.

Q55. An 8-to-1 MUX needs

A) 2

B) 3

C) 4

D) 8

Answer: B) 3
Explanation: $2^3 = 8$.

Q56. DEMUX stands for

A) Demultiplexer

B) Digital Multiplexer

C) Decoder Multiplexer

D) Data Memory Unit

Answer: A) Demultiplexer
Explanation: It distributes one input.

Q57. A 1-to-4 DEMUX has

A) 1 input and 4 outputs

B) 4 inputs and 1 output

C) 2 inputs and 4 outputs

D) 4 and 4

Answer: A) 1 input and 4 outputs
Explanation: One data input, four outputs.

Q58. A decoder converts

A) n inputs to up to 2■ outputs

B) 2■ inputs to n outputs

C) Analog to digital

D) Digital to analog

Answer: A) n inputs to up to 2■ outputs
Explanation: Decoder expands coded inputs.

Q59. An encoder performs the reverse of

A) Decoder

B) Adder

C) Counter

D) Register

Answer: A) Decoder
Explanation: Encoder converts active input to code.

Q60. An 8-to-3 encoder has

A) 8 inputs and 3 outputs

B) 3 inputs and 8 outputs

C) 8 and 8

D) 3 and 3

Answer: A) 8 inputs and 3 outputs
Explanation: It encodes eight inputs into three bits.

Q61. A flip-flop stores

A) One bit

B) One byte

C) Four bytes

D) No information

Answer: A) One bit
Explanation: It is a one-bit storage element.

Q62. JK flip-flop with J=K=1

A) Sets

B) Resets

C) Toggles

D) Holds

Answer: C) Toggles
Explanation: JK toggles when both are 1.

Q63. JK flip-flop with J=K=0

A) Sets

B) Resets

C) Toggles

D) Holds

Answer: D) Holds
Explanation: No change.

Q64. D flip-flop is also called

A) Data flip-flop

B) Digital counter

C) Delay flip-flop

D) Both A and C

Answer: D) Both A and C
Explanation: D commonly means data/delay.

Q65. T flip-flop is used for

A) Toggling

B) Decoding

C) Encoding

D) Multiplexing

Answer: A) Toggling
Explanation: T=1 causes toggling.

Q66. Race-around occurs mainly in

A) Level-triggered JK

B) D flip-flop

C) T only

D) Register

Answer: A) Level-triggered JK
Explanation: It occurs with J=K=1 and a long clock pulse.

Q67. Race-around can be avoided by

A) Master-slave configuration

B) More inputs

C) Higher voltage

D) Decoder

Answer: A) Master-slave configuration
Explanation: Master-slave operation prevents repeated toggling.

Q68. Positive edge means

A) 1 to 0

B) 0 to 1

C) Constant 1

D) Constant 0

Answer: B) 0 to 1
Explanation: Positive edge is rising edge.

Q69. Negative edge means

A) 0 to 1

B) 1 to 0

C) Constant 1

D) Constant 0

Answer: B) 1 to 0
Explanation: Negative edge is falling edge.

Q70. Setup time is measured

A) Before clock edge

B) After clock edge

C) Before power off

D) After reset only

Answer: A) Before clock edge
Explanation: Data must be stable before the edge.

Q71. A register is a group of

A) Flip-flops

B) Gates only

C) Counters only

D) Decoders

Answer: A) Flip-flops
Explanation: Each flip-flop stores one bit.

Q72. SISO stands for

A) Serial In Serial Out

B) Serial In Parallel Out

C) Parallel In Serial Out

D) Parallel In Parallel Out

Answer: A) Serial In Serial Out
Explanation: SISO shifts serially in and out.

Q73. SIPO stands for

A) Serial In Parallel Out

B) Serial In Serial Out

C) Parallel In Serial Out

D) Parallel In Parallel Out

Answer: A) Serial In Parallel Out
Explanation: Serial input becomes parallel output.

Q74. PISO stands for

A) Parallel In Serial Out

B) Parallel In Parallel Out

C) Serial In Parallel Out

D) Serial In Serial Out

Answer: A) Parallel In Serial Out
Explanation: Parallel data is shifted out serially.

Q75. PIPO stands for

A) Parallel In Parallel Out

B) Parallel In Serial Out

C) Serial In Parallel Out

D) Serial In Serial Out

Answer: A) Parallel In Parallel Out
Explanation: Both input and output are parallel.

Q76. A universal shift register can

A) Shift both directions and parallel load

B) Only serial input

C) Only serial output

D) Only count

Answer: A) Shift both directions and parallel load
Explanation: It supports multiple modes.

Q77. A 4-bit register stores

A) 2 bits

B) 4 bits

C) 8 bits

D) 16 bits

Answer: B) 4 bits
Explanation: Four flip-flops store four bits.

Q78. A ring counter is based on

A) Shift register

B) MUX

C) Decoder

D) Adder

Answer: A) Shift register
Explanation: It uses shift-register feedback.

Q79. A Johnson counter is also called

A) Twisted ring counter

B) Ripple counter

C) Binary counter

D) Decade counter

Answer: A) Twisted ring counter
Explanation: It uses complemented feedback.

Q80. A 4-bit Johnson counter has

A) 4

B) 8

C) 16

D) 32

Answer: B) 8
Explanation: 2n = 8 states.

Q81. A counter is a

A) Sequential circuit

B) Combinational circuit

C) Analog circuit

D) Decoder

Answer: A) Sequential circuit
Explanation: Counters use memory.

Q82. An asynchronous counter is also called

A) Ripple counter

B) Synchronous counter

C) Ring counter

D) Johnson counter

Answer: A) Ripple counter
Explanation: Clock ripples through stages.

Q83. A synchronous counter has

A) Common clock

B) Different clocks always

C) No clock

D) Analog clock

Answer: A) Common clock
Explanation: All stages receive the clock.

Q84. A 3-bit binary counter has

A) 3

B) 6

C) 8

D) 16

Answer: C) 8
Explanation: $2^3 = 8$ states.

Q85. A 4-bit binary counter has

A) 4

B) 8

C) 16

D) 32

Answer: C) 16
Explanation: 2■ = 16 states.

Q86. A MOD-10 counter is called

A) Decade counter

B) Binary counter

C) Ring counter

D) Johnson counter

Answer: A) Decade counter
Explanation: It has ten states.

Q87. A MOD-8 counter needs

A) 2

B) 3

C) 4

D) 8

Answer: B) 3
Explanation: $2^3 = 8$.

Q88. A MOD-16 counter needs

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: 2■ = 16.

Q89. An up counter counts

A) Increasing sequence

B) Decreasing sequence

C) Random sequence

D) No sequence

Answer: A) Increasing sequence
Explanation: It increments.

Q90. An up/down counter counts

A) Both directions

B) Only up

C) Only down

D) Neither

Answer: A) Both directions
Explanation: Direction is selectable.

Q91. RAM stands for

A) Random Access Memory

B) Read Access Module

C) Rapid Access Machine

D) Random Arithmetic Memory

Answer: A) Random Access Memory
Explanation: RAM permits random access.

Q92. ROM stands for

A) Read Only Memory

B) Random Output Memory

C) Read Output Module

D) Register Only Memory

Answer: A) Read Only Memory
Explanation: ROM is read-only in normal operation.

Q93. RAM is generally

A) Volatile

B) Non-volatile

C) Permanent

D) Mechanical

Answer: A) Volatile
Explanation: RAM loses data without power.

Q94. ROM is generally

A) Volatile

B) Non-volatile

C) Temporary

D) Dynamic only

Answer: B) Non-volatile
Explanation: ROM retains data.

Q95. SRAM stands for

A) Static RAM

B) Serial RAM

C) System RAM

D) Standard RAM

Answer: A) Static RAM
Explanation: Static random-access memory.

Q96. DRAM stands for

A) Dynamic RAM

B) Digital RAM

C) Direct RAM

D) Dual RAM

Answer: A) Dynamic RAM
Explanation: Dynamic random-access memory.

Q97. DRAM requires

A) Refreshing

B) Encoding

C) Decoding

D) Counting

Answer: A) Refreshing
Explanation: Its capacitor charge leaks.

Q98. PROM stands for

A) Programmable Read Only Memory

B) Parallel Read Only Memory

C) Primary ROM

D) Programmable RAM

Answer: A) Programmable Read Only Memory
Explanation: PROM can be programmed once.

Q99. EPROM can be erased using

A) Ultraviolet light

B) Sound

C) Heat only

D) Magnetic field

Answer: A) Ultraviolet light
Explanation: Traditional EPROM uses UV erasure.

Q100. EEPROM can be erased

A) Electrically

B) Only by UV

C) Mechanically

D) Magnetically

Answer: A) Electrically
Explanation: EEPROM is electrically erasable.

UNIT 3: K-Map & Boolean Functions

Q101. TTL stands for

A) Transistor-Transistor Logic

B) Transistor Transfer Logic

C) Total Transistor Logic

D) Two Transistor Logic

Answer: A) Transistor-Transistor Logic
Explanation: TTL is a bipolar logic family.

Q102. CMOS stands for

A) Complementary Metal-Oxide-Semiconductor

B) Common Metal Oxide System

C) Complementary Memory Operating System

D) Current Metal Operating Semiconductor

Answer: A) Complementary Metal-Oxide-Semiconductor
Explanation: CMOS uses complementary MOS devices.

Q103. CMOS has generally

A) Low static power

B) Very high static power

C) No logic

D) No switching

Answer: A) Low static power
Explanation: Low static power is a key advantage.

Q104. TTL primarily uses

A) Bipolar transistors

B) MOSFETs only

C) Vacuum tubes

D) Relays

Answer: A) Bipolar transistors
Explanation: Traditional TTL uses BJTs.

Q105. CMOS primarily uses

A) MOSFETs

B) BJTs only

C) Relays

D) Diodes only

Answer: A) MOSFETs
Explanation: CMOS uses MOS transistors.

Q106. Fan-out refers to

A) Number of inputs a gate output can drive

B) Number of power supplies

C) Number of clocks

D) Memory outputs

Answer: A) Number of inputs a gate output can drive
Explanation: It is load-driving capability.

Q107. Propagation delay is

A) Input-to-output response delay

B) Power-to-clock delay

C) Two-clock delay

D) Reset-to-power delay

Answer: A) Input-to-output response delay
Explanation: It measures switching response.

Q108. Noise margin indicates

A) Tolerance against noise

B) Power consumption

C) Clock speed

D) Memory size

Answer: A) Tolerance against noise
Explanation: Higher margin improves noise immunity.

Q109. ADC stands for

A) Analog-to-Digital Converter

B) Automatic Digital Counter

C) Analog Data Circuit

D) Advanced Digital Controller

Answer: A) Analog-to-Digital Converter
Explanation: ADC digitizes analog signals.

Q110. DAC stands for

A) Digital-to-Analog Converter

B) Data Analog Counter

C) Digital Arithmetic Circuit

D) Direct Analog Controller

Answer: A) Digital-to-Analog Converter
Explanation: DAC produces analog output from digital code.

Q111. The decimal value of hexadecimal F is

A) 13

B) 14

C) 15

D) 16

Answer: C) 15
Explanation: F■■ = 15.

Q112. A + 1 equals

A) A

B) 0

C) 1

D) A'

Answer: C) 1
Explanation: Dominance law.

Q113. A 5-variable K-map contains

A) 8 cells

B) 16 cells

C) 32 cells

D) 64 cells

Answer: C) 32 cells
Explanation: 2■ = 32.

Q114. The sum output of a half adder uses

A) AND

B) OR

C) XOR

D) NOR

Answer: C) XOR
Explanation: S = A XOR B.

Q115. A 16-to-1 MUX needs

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: 2■ = 16.

Q116. A T flip-flop with T=0

A) Holds

B) Toggles

C) Sets

D) Resets

Answer: A) Holds
Explanation: T=0 means no change.

Q117. A 16-bit register requires

A) 8 flip-flops

B) 16 flip-flops

C) 32 flip-flops

D) 4 flip-flops

Answer: B) 16 flip-flops
Explanation: One flip-flop stores one bit.

Q118. A MOD-6 counter needs at least

A) 2 flip-flops

B) 3 flip-flops

C) 4 flip-flops

D) 6 flip-flops

Answer: B) 3 flip-flops
Explanation: $2^3 = 8$, enough for 6 states.

Q119. SRAM is generally

A) Faster than DRAM

B) Slower than DRAM always

C) Non-memory

D) Analog

Answer: A) Faster than DRAM
Explanation: SRAM avoids refresh and is typically faster.

Q120. CMOS is known for

A) Low static power

B) High static power

C) No input impedance

D) No switching

Answer: A) Low static power
Explanation: CMOS draws little static power.

Q121. A binary digit is called a (Practice variation 2)

A) Byte

B) Bit

C) Nibble

D) Word

Answer: B) Bit
Explanation: A bit is one binary digit.

Q122. A · 0 equals (Practice variation 2)

A) A

B) 0

C) 1

D) A'

Answer: B) 0
Explanation: An AND with 0 is 0.

Q123. A group of 4 K-map cells eliminates (Practice variation 2)

A) 1 variable

B) 2 variables

C) 3 variables

D) 4 variables

Answer: B) 2 variables
Explanation: Each doubling of group size removes one variable.

Q124. The carry output of a half adder uses (Practice variation 2)

A) AND

B) OR

C) XOR

D) NOT

Answer: A) AND
Explanation: C = AB.

Q125. A 1-to-16 DEMUX needs (Practice variation 2)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: Four select lines choose one of 16 outputs.

Q126. A T flip-flop with T=1 (Practice variation 2)

A) Holds

B) Toggles

C) Sets only

D) Resets only

Answer: B) Toggles
Explanation: T=1 complements the state.

Q127. SIPO converts (Practice variation 2)

A) Serial to parallel

B) Parallel to serial

C) Analog to digital

D) Digital to analog

Answer: A) Serial to parallel
Explanation: SIPO expands serial data into parallel form.

Q128. A MOD-10 counter needs at least (Practice variation 2)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: 2■ = 16, enough for 10.

Q129. DRAM stores charge mainly in a (Practice variation 2)

A) Capacitor

B) Transformer

C) Relay

D) Decoder

Answer: A) Capacitor
Explanation: A DRAM cell uses a capacitor.

Q130. Fan-in means (Practice variation 2)

A) Number of gate inputs

B) Number of loads

C) Memory size

D) Clock frequency

Answer: A) Number of gate inputs
Explanation: Fan-in is input count.

Q131. The range of an unsigned 4-bit number is (Practice variation 3)

A) 0–7

B) 0–15

C) –8 to 7

D) 1–16

Answer: B) 0–15
Explanation: There are 16 values from 0 to 15.

Q132. A + A' equals (Practice variation 3)

A) A

B) 0

C) 1

D) A'

Answer: C) 1
Explanation: Complement law.

Q133. Don't-care conditions are commonly represented by (Practice variation 3)

A) X

B) Z

C) Y

D) D

Answer: A) X
Explanation: X denotes either 0 or 1 for minimization.

Q134. A full adder has (Practice variation 3)

A) 2 inputs

B) 3 inputs

C) 4 inputs

D) 5 inputs

Answer: B) 3 inputs
Explanation: A, B and Cin.

Q135. A 3-to-8 decoder has (Practice variation 3)

A) 3 outputs

B) 6 outputs

C) 8 outputs

D) 16 outputs

Answer: C) 8 outputs
Explanation: $2^3 = 8$.

Q136. A D flip-flop is commonly used in (Practice variation 3)

A) Registers

B) Transformers

C) Amplifiers

D) Filters

Answer: A) Registers
Explanation: D flip-flops form registers.

Q137. PISO converts (Practice variation 3)

A) Parallel to serial

B) Serial to parallel

C) Analog to digital

D) Digital to analog

Answer: A) Parallel to serial
Explanation: PISO shifts parallel-loaded data out serially.

Q138. A 3-bit binary counter has (Practice variation 3)

A) 4

B) 6

C) 8

D) 16

Answer: C) 8
Explanation: $2^3 = 8$ states.

Q139. EPROM is traditionally erased using (Practice variation 3)

A) UV light

B) Electrical pulse only

C) Sound

D) Magnetic field

Answer: A) UV light
Explanation: UV light erases floating-gate EPROM.

Q140. Rise time describes transition from (Practice variation 3)

A) Low to high

B) High to low

C) High to high

D) Low to low

Answer: A) Low to high
Explanation: It is the low-to-high transition time.

Q141. The range of signed 4-bit two's-complement numbers is (Practice variation 4)

A) 0–15

B) –7 to 7

C) –8 to 7

D) –15 to 15

Answer: C) –8 to 7
Explanation: The range is -2^3 to 2^3-1.

Q142. A · A' equals (Practice variation 4)

A) A

B) 0

C) 1

D) A'

Answer: B) 0
Explanation: Complement law.

Q143. Canonical SOP uses (Practice variation 4)

A) Minterms

B) Maxterms

C) Registers

D) Counters

Answer: A) Minterms
Explanation: SOP is expressed as a sum of minterms.

Q144. A comparator indicates (Practice variation 4)

A) A>B, A=B, A<B

B) Only A>B

C) Only equality

D) Only A<B

Answer: A) A>B, A=B, A<B
Explanation: A magnitude comparator gives three relations.

Q145. A 8-to-3 encoder has (Practice variation 4)

A) 8 inputs and 3 outputs

B) 3 inputs and 8 outputs

C) 8 and 8

D) 3 and 3

Answer: A) 8 inputs and 3 outputs
Explanation: It compresses one-of-eight input to 3 bits.

Q146. Setup time is the time data must be stable (Practice variation 4)

A) Before active clock edge

B) After active edge

C) Before power off

D) After reset only

Answer: A) Before active clock edge
Explanation: Setup precedes the sampling edge.

Q147. A ring counter uses (Practice variation 4)

A) Feedback

B) No feedback

C) Only analog input

D) Only a decoder

Answer: A) Feedback
Explanation: The last stage feeds the first.

Q148. A 4-bit counter divides the input frequency at its MSB by (Practice variation 4)

A) 4

B) 8

C) 16

D) 32

Answer: C) 16
Explanation: Each stage divides by 2.

Q149. FPGA stands for (Practice variation 4)

A) Field Programmable Gate Array

B) Fast Programmable Gate Array

C) Field Processing Gate Array

D) Fixed Programmable Gate Array

Answer: A) Field Programmable Gate Array
Explanation: FPGA is a programmable logic device.

Q150. Fall time describes transition from (Practice variation 4)

A) High to low

B) Low to high

C) Low to low

D) High to high

Answer: A) High to low
Explanation: It is the high-to-low transition time.

UNIT 4: Adders, Subtractors & Comparators

Q151. Which code is commonly used in shaft encoders? (Practice variation 5)

A) BCD

B) Gray

C) ASCII

D) Excess-3

Answer: B) Gray
Explanation: Gray code minimizes transition ambiguity.

Q152. Which gate is mainly used for parity checking? (Practice variation 5)

A) AND

B) OR

C) XOR

D) NOT

Answer: C) XOR
Explanation: XOR naturally detects odd parity.

Q153. Canonical POS uses (Practice variation 5)

A) Minterms

B) Maxterms

C) Flip-flops

D) Encoders

Answer: B) Maxterms
Explanation: POS is expressed as a product of maxterms.

Q154. A carry look-ahead adder is faster mainly because it (Practice variation 5)

A) Computes carry in parallel

B) Uses no gates

C) Stores carry

D) Uses analog signals

Answer: A) Computes carry in parallel
Explanation: Parallel carry computation reduces delay.

Q155. A BCD-to-7-segment circuit is a (Practice variation 5)

A) Decoder

B) Encoder

C) Adder

D) Counter

Answer: A) Decoder
Explanation: It decodes BCD into display segments.

Q156. Hold time is the time data must remain stable (Practice variation 5)

A) After active clock edge

B) Before active edge

C) Before power off

D) During reset only

Answer: A) After active clock edge
Explanation: Hold follows the sampling edge.

Q157. A 4-bit Johnson counter has (Practice variation 5)

A) 4

B) 8

C) 16

D) 32

Answer: B) 8
Explanation: A Johnson counter has 2n states.

Q158. A synchronous counter uses (Practice variation 5)

A) A common clock

B) Ripple clocks only

C) No clock

D) Analog clock

Answer: A) A common clock
Explanation: All flip-flops are clocked together.

Q159. PLA has programmable (Practice variation 5)

A) AND and OR arrays

B) Only OR array

C) Only AND array

D) Only flip-flops

Answer: A) AND and OR arrays
Explanation: Both planes are programmable in a PLA.

Q160. An 8-bit ADC has (Practice variation 5)

A) 128

B) 256

C) 512

D) 1024

Answer: B) 256
Explanation: 2■ = 256 quantization levels.

Q161. The decimal value of hexadecimal F is (Practice variation 6)

A) 13

B) 14

C) 15

D) 16

Answer: C) 15
Explanation: F■■ = 15.

Q162. A + 1 equals (Practice variation 6)

A) A

B) 0

C) 1

D) A'

Answer: C) 1
Explanation: Dominance law.

Q163. A 5-variable K-map contains (Practice variation 6)

A) 8 cells

B) 16 cells

C) 32 cells

D) 64 cells

Answer: C) 32 cells
Explanation: 2■ = 32.

Q164. The sum output of a half adder uses (Practice variation 6)

A) AND

B) OR

C) XOR

D) NOR

Answer: C) XOR
Explanation: S = A XOR B.

Q165. A 16-to-1 MUX needs (Practice variation 6)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: 2■ = 16.

Q166. A T flip-flop with T=0 (Practice variation 6)

A) Holds

B) Toggles

C) Sets

D) Resets

Answer: A) Holds
Explanation: T=0 means no change.

Q167. A 16-bit register requires (Practice variation 6)

A) 8 flip-flops

B) 16 flip-flops

C) 32 flip-flops

D) 4 flip-flops

Answer: B) 16 flip-flops
Explanation: One flip-flop stores one bit.

Q168. A MOD-6 counter needs at least (Practice variation 6)

A) 2 flip-flops

B) 3 flip-flops

C) 4 flip-flops

D) 6 flip-flops

Answer: B) 3 flip-flops
Explanation: $2^3 = 8$, enough for 6 states.

Q169. SRAM is generally (Practice variation 6)

A) Faster than DRAM

B) Slower than DRAM always

C) Non-memory

D) Analog

Answer: A) Faster than DRAM
Explanation: SRAM avoids refresh and is typically faster.

Q170. CMOS is known for (Practice variation 6)

A) Low static power

B) High static power

C) No input impedance

D) No switching

Answer: A) Low static power
Explanation: CMOS draws little static power.

Q171. A binary digit is called a (Practice variation 7)

A) Byte

B) Bit

C) Nibble

D) Word

Answer: B) Bit
Explanation: A bit is one binary digit.

Q172. A · 0 equals (Practice variation 7)

A) A

B) 0

C) 1

D) A'

Answer: B) 0
Explanation: An AND with 0 is 0.

Q173. A group of 4 K-map cells eliminates (Practice variation 7)

A) 1 variable

B) 2 variables

C) 3 variables

D) 4 variables

Answer: B) 2 variables
Explanation: Each doubling of group size removes one variable.

Q174. The carry output of a half adder uses (Practice variation 7)

A) AND

B) OR

C) XOR

D) NOT

Answer: A) AND
Explanation: C = AB.

Q175. A 1-to-16 DEMUX needs (Practice variation 7)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: Four select lines choose one of 16 outputs.

Q176. A T flip-flop with T=1 (Practice variation 7)

A) Holds

B) Toggles

C) Sets only

D) Resets only

Answer: B) Toggles
Explanation: T=1 complements the state.

Q177. SIPO converts (Practice variation 7)

A) Serial to parallel

B) Parallel to serial

C) Analog to digital

D) Digital to analog

Answer: A) Serial to parallel
Explanation: SIPO expands serial data into parallel form.

Q178. A MOD-10 counter needs at least (Practice variation 7)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: 2■ = 16, enough for 10.

Q179. DRAM stores charge mainly in a (Practice variation 7)

A) Capacitor

B) Transformer

C) Relay

D) Decoder

Answer: A) Capacitor
Explanation: A DRAM cell uses a capacitor.

Q180. Fan-in means (Practice variation 7)

A) Number of gate inputs

B) Number of loads

C) Memory size

D) Clock frequency

Answer: A) Number of gate inputs
Explanation: Fan-in is input count.

Q181. The range of an unsigned 4-bit number is (Practice variation 8)

A) 0–7

B) 0–15

C) –8 to 7

D) 1–16

Answer: B) 0–15
Explanation: There are 16 values from 0 to 15.

Q182. A + A' equals (Practice variation 8)

A) A

B) 0

C) 1

D) A'

Answer: C) 1
Explanation: Complement law.

Q183. Don't-care conditions are commonly represented by (Practice variation 8)

A) X

B) Z

C) Y

D) D

Answer: A) X
Explanation: X denotes either 0 or 1 for minimization.

Q184. A full adder has (Practice variation 8)

A) 2 inputs

B) 3 inputs

C) 4 inputs

D) 5 inputs

Answer: B) 3 inputs
Explanation: A, B and Cin.

Q185. A 3-to-8 decoder has (Practice variation 8)

A) 3 outputs

B) 6 outputs

C) 8 outputs

D) 16 outputs

Answer: C) 8 outputs
Explanation: $2^3 = 8$.

Q186. A D flip-flop is commonly used in (Practice variation 8)

A) Registers

B) Transformers

C) Amplifiers

D) Filters

Answer: A) Registers
Explanation: D flip-flops form registers.

Q187. PISO converts (Practice variation 8)

A) Parallel to serial

B) Serial to parallel

C) Analog to digital

D) Digital to analog

Answer: A) Parallel to serial
Explanation: PISO shifts parallel-loaded data out serially.

Q188. A 3-bit binary counter has (Practice variation 8)

A) 4

B) 6

C) 8

D) 16

Answer: C) 8
Explanation: $2^3 = 8$ states.

Q189. EPROM is traditionally erased using (Practice variation 8)

A) UV light

B) Electrical pulse only

C) Sound

D) Magnetic field

Answer: A) UV light
Explanation: UV light erases floating-gate EPROM.

Q190. Rise time describes transition from (Practice variation 8)

A) Low to high

B) High to low

C) High to high

D) Low to low

Answer: A) Low to high
Explanation: It is the low-to-high transition time.

Q191. The range of signed 4-bit two's-complement numbers is (Practice variation 9)

A) 0–15

B) –7 to 7

C) –8 to 7

D) –15 to 15

Answer: C) –8 to 7
Explanation: The range is -2^3 to 2^3-1.

Q192. A · A' equals (Practice variation 9)

A) A

B) 0

C) 1

D) A'

Answer: B) 0
Explanation: Complement law.

Q193. Canonical SOP uses (Practice variation 9)

A) Minterms

B) Maxterms

C) Registers

D) Counters

Answer: A) Minterms
Explanation: SOP is expressed as a sum of minterms.

Q194. A comparator indicates (Practice variation 9)

A) A>B, A=B, A<B

B) Only A>B

C) Only equality

D) Only A<B

Answer: A) A>B, A=B, A<B
Explanation: A magnitude comparator gives three relations.

Q195. A 8-to-3 encoder has (Practice variation 9)

A) 8 inputs and 3 outputs

B) 3 inputs and 8 outputs

C) 8 and 8

D) 3 and 3

Answer: A) 8 inputs and 3 outputs
Explanation: It compresses one-of-eight input to 3 bits.

Q196. Setup time is the time data must be stable (Practice variation 9)

A) Before active clock edge

B) After active edge

C) Before power off

D) After reset only

Answer: A) Before active clock edge
Explanation: Setup precedes the sampling edge.

Q197. A ring counter uses (Practice variation 9)

A) Feedback

B) No feedback

C) Only analog input

D) Only a decoder

Answer: A) Feedback
Explanation: The last stage feeds the first.

Q198. A 4-bit counter divides the input frequency at its MSB by (Practice variation 9)

A) 4

B) 8

C) 16

D) 32

Answer: C) 16
Explanation: Each stage divides by 2.

Q199. FPGA stands for (Practice variation 9)

A) Field Programmable Gate Array

B) Fast Programmable Gate Array

C) Field Processing Gate Array

D) Fixed Programmable Gate Array

Answer: A) Field Programmable Gate Array
Explanation: FPGA is a programmable logic device.

Q200. Fall time describes transition from (Practice variation 9)

A) High to low

B) Low to high

C) Low to low

D) High to high

Answer: A) High to low
Explanation: It is the high-to-low transition time.

UNIT 5: MUX, DEMUX, Encoder & Decoder

Q201. Which code is commonly used in shaft encoders? (Practice variation 10)

A) BCD

B) Gray

C) ASCII

D) Excess-3

Answer: B) Gray
Explanation: Gray code minimizes transition ambiguity.

Q202. Which gate is mainly used for parity checking? (Practice variation 10)

A) AND

B) OR

C) XOR

D) NOT

Answer: C) XOR
Explanation: XOR naturally detects odd parity.

Q203. Canonical POS uses (Practice variation 10)

A) Minterms

B) Maxterms

C) Flip-flops

D) Encoders

Answer: B) Maxterms
Explanation: POS is expressed as a product of maxterms.

Q204. A carry look-ahead adder is faster mainly because it (Practice variation 10)

A) Computes carry in parallel

B) Uses no gates

C) Stores carry

D) Uses analog signals

Answer: A) Computes carry in parallel
Explanation: Parallel carry computation reduces delay.

Q205. A BCD-to-7-segment circuit is a (Practice variation 10)

A) Decoder

B) Encoder

C) Adder

D) Counter

Answer: A) Decoder
Explanation: It decodes BCD into display segments.

Q206. Hold time is the time data must remain stable (Practice variation 10)

A) After active clock edge

B) Before active edge

C) Before power off

D) During reset only

Answer: A) After active clock edge
Explanation: Hold follows the sampling edge.

Q207. A 4-bit Johnson counter has (Practice variation 10)

A) 4

B) 8

C) 16

D) 32

Answer: B) 8
Explanation: A Johnson counter has 2n states.

Q208. A synchronous counter uses (Practice variation 10)

A) A common clock

B) Ripple clocks only

C) No clock

D) Analog clock

Answer: A) A common clock
Explanation: All flip-flops are clocked together.

Q209. PLA has programmable (Practice variation 10)

A) AND and OR arrays

B) Only OR array

C) Only AND array

D) Only flip-flops

Answer: A) AND and OR arrays
Explanation: Both planes are programmable in a PLA.

Q210. An 8-bit ADC has (Practice variation 10)

A) 128

B) 256

C) 512

D) 1024

Answer: B) 256
Explanation: 2■ = 256 quantization levels.

Q211. The decimal value of hexadecimal F is (Practice variation 11)

A) 13

B) 14

C) 15

D) 16

Answer: C) 15
Explanation: F■■ = 15.

Q212. A + 1 equals (Practice variation 11)

A) A

B) 0

C) 1

D) A'

Answer: C) 1
Explanation: Dominance law.

Q213. A 5-variable K-map contains (Practice variation 11)

A) 8 cells

B) 16 cells

C) 32 cells

D) 64 cells

Answer: C) 32 cells
Explanation: 2■ = 32.

Q214. The sum output of a half adder uses (Practice variation 11)

A) AND

B) OR

C) XOR

D) NOR

Answer: C) XOR
Explanation: S = A XOR B.

Q215. A 16-to-1 MUX needs (Practice variation 11)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: 2■ = 16.

Q216. A T flip-flop with T=0 (Practice variation 11)

A) Holds

B) Toggles

C) Sets

D) Resets

Answer: A) Holds
Explanation: T=0 means no change.

Q217. A 16-bit register requires (Practice variation 11)

A) 8 flip-flops

B) 16 flip-flops

C) 32 flip-flops

D) 4 flip-flops

Answer: B) 16 flip-flops
Explanation: One flip-flop stores one bit.

Q218. A MOD-6 counter needs at least (Practice variation 11)

A) 2 flip-flops

B) 3 flip-flops

C) 4 flip-flops

D) 6 flip-flops

Answer: B) 3 flip-flops
Explanation: $2^3 = 8$, enough for 6 states.

Q219. SRAM is generally (Practice variation 11)

A) Faster than DRAM

B) Slower than DRAM always

C) Non-memory

D) Analog

Answer: A) Faster than DRAM
Explanation: SRAM avoids refresh and is typically faster.

Q220. CMOS is known for (Practice variation 11)

A) Low static power

B) High static power

C) No input impedance

D) No switching

Answer: A) Low static power
Explanation: CMOS draws little static power.

Q221. A binary digit is called a (Practice variation 12)

A) Byte

B) Bit

C) Nibble

D) Word

Answer: B) Bit
Explanation: A bit is one binary digit.

Q222. A · 0 equals (Practice variation 12)

A) A

B) 0

C) 1

D) A'

Answer: B) 0
Explanation: An AND with 0 is 0.

Q223. A group of 4 K-map cells eliminates (Practice variation 12)

A) 1 variable

B) 2 variables

C) 3 variables

D) 4 variables

Answer: B) 2 variables
Explanation: Each doubling of group size removes one variable.

Q224. The carry output of a half adder uses (Practice variation 12)

A) AND

B) OR

C) XOR

D) NOT

Answer: A) AND
Explanation: C = AB.

Q225. A 1-to-16 DEMUX needs (Practice variation 12)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: Four select lines choose one of 16 outputs.

Q226. A T flip-flop with T=1 (Practice variation 12)

A) Holds

B) Toggles

C) Sets only

D) Resets only

Answer: B) Toggles
Explanation: T=1 complements the state.

Q227. SIPO converts (Practice variation 12)

A) Serial to parallel

B) Parallel to serial

C) Analog to digital

D) Digital to analog

Answer: A) Serial to parallel
Explanation: SIPO expands serial data into parallel form.

Q228. A MOD-10 counter needs at least (Practice variation 12)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: 2■ = 16, enough for 10.

Q229. DRAM stores charge mainly in a (Practice variation 12)

A) Capacitor

B) Transformer

C) Relay

D) Decoder

Answer: A) Capacitor
Explanation: A DRAM cell uses a capacitor.

Q230. Fan-in means (Practice variation 12)

A) Number of gate inputs

B) Number of loads

C) Memory size

D) Clock frequency

Answer: A) Number of gate inputs
Explanation: Fan-in is input count.

Q231. The range of an unsigned 4-bit number is (Practice variation 13)

A) 0–7

B) 0–15

C) –8 to 7

D) 1–16

Answer: B) 0–15
Explanation: There are 16 values from 0 to 15.

Q232. A + A' equals (Practice variation 13)

A) A

B) 0

C) 1

D) A'

Answer: C) 1
Explanation: Complement law.

Q233. Don't-care conditions are commonly represented by (Practice variation 13)

A) X

B) Z

C) Y

D) D

Answer: A) X
Explanation: X denotes either 0 or 1 for minimization.

Q234. A full adder has (Practice variation 13)

A) 2 inputs

B) 3 inputs

C) 4 inputs

D) 5 inputs

Answer: B) 3 inputs
Explanation: A, B and Cin.

Q235. A 3-to-8 decoder has (Practice variation 13)

A) 3 outputs

B) 6 outputs

C) 8 outputs

D) 16 outputs

Answer: C) 8 outputs
Explanation: $2^3 = 8$.

Q236. A D flip-flop is commonly used in (Practice variation 13)

A) Registers

B) Transformers

C) Amplifiers

D) Filters

Answer: A) Registers
Explanation: D flip-flops form registers.

Q237. PISO converts (Practice variation 13)

A) Parallel to serial

B) Serial to parallel

C) Analog to digital

D) Digital to analog

Answer: A) Parallel to serial
Explanation: PISO shifts parallel-loaded data out serially.

Q238. A 3-bit binary counter has (Practice variation 13)

A) 4

B) 6

C) 8

D) 16

Answer: C) 8
Explanation: $2^3 = 8$ states.

Q239. EPROM is traditionally erased using (Practice variation 13)

A) UV light

B) Electrical pulse only

C) Sound

D) Magnetic field

Answer: A) UV light
Explanation: UV light erases floating-gate EPROM.

Q240. Rise time describes transition from (Practice variation 13)

A) Low to high

B) High to low

C) High to high

D) Low to low

Answer: A) Low to high
Explanation: It is the low-to-high transition time.

Q241. The range of signed 4-bit two's-complement numbers is (Practice variation 14)

A) 0–15

B) –7 to 7

C) –8 to 7

D) –15 to 15

Answer: C) –8 to 7
Explanation: The range is -2^3 to 2^3-1.

Q242. A · A' equals (Practice variation 14)

A) A

B) 0

C) 1

D) A'

Answer: B) 0
Explanation: Complement law.

Q243. Canonical SOP uses (Practice variation 14)

A) Minterms

B) Maxterms

C) Registers

D) Counters

Answer: A) Minterms
Explanation: SOP is expressed as a sum of minterms.

Q244. A comparator indicates (Practice variation 14)

A) A>B, A=B, A<B

B) Only A>B

C) Only equality

D) Only A<B

Answer: A) A>B, A=B, A<B
Explanation: A magnitude comparator gives three relations.

Q245. A 8-to-3 encoder has (Practice variation 14)

A) 8 inputs and 3 outputs

B) 3 inputs and 8 outputs

C) 8 and 8

D) 3 and 3

Answer: A) 8 inputs and 3 outputs
Explanation: It compresses one-of-eight input to 3 bits.

Q246. Setup time is the time data must be stable (Practice variation 14)

A) Before active clock edge

B) After active edge

C) Before power off

D) After reset only

Answer: A) Before active clock edge
Explanation: Setup precedes the sampling edge.

Q247. A ring counter uses (Practice variation 14)

A) Feedback

B) No feedback

C) Only analog input

D) Only a decoder

Answer: A) Feedback
Explanation: The last stage feeds the first.

Q248. A 4-bit counter divides the input frequency at its MSB by (Practice variation 14)

A) 4

B) 8

C) 16

D) 32

Answer: C) 16
Explanation: Each stage divides by 2.

Q249. FPGA stands for (Practice variation 14)

A) Field Programmable Gate Array

B) Fast Programmable Gate Array

C) Field Processing Gate Array

D) Fixed Programmable Gate Array

Answer: A) Field Programmable Gate Array
Explanation: FPGA is a programmable logic device.

Q250. Fall time describes transition from (Practice variation 14)

A) High to low

B) Low to high

C) Low to low

D) High to high

Answer: A) High to low
Explanation: It is the high-to-low transition time.

UNIT 6: Latches & Flip-Flops

Q251. Which code is commonly used in shaft encoders? (Practice variation 15)

A) BCD

B) Gray

C) ASCII

D) Excess-3

Answer: B) Gray
Explanation: Gray code minimizes transition ambiguity.

Q252. Which gate is mainly used for parity checking? (Practice variation 15)

A) AND

B) OR

C) XOR

D) NOT

Answer: C) XOR
Explanation: XOR naturally detects odd parity.

Q253. Canonical POS uses (Practice variation 15)

A) Minterms

B) Maxterms

C) Flip-flops

D) Encoders

Answer: B) Maxterms
Explanation: POS is expressed as a product of maxterms.

Q254. A carry look-ahead adder is faster mainly because it (Practice variation 15)

A) Computes carry in parallel

B) Uses no gates

C) Stores carry

D) Uses analog signals

Answer: A) Computes carry in parallel
Explanation: Parallel carry computation reduces delay.

Q255. A BCD-to-7-segment circuit is a (Practice variation 15)

A) Decoder

B) Encoder

C) Adder

D) Counter

Answer: A) Decoder
Explanation: It decodes BCD into display segments.

Q256. Hold time is the time data must remain stable (Practice variation 15)

A) After active clock edge

B) Before active edge

C) Before power off

D) During reset only

Answer: A) After active clock edge
Explanation: Hold follows the sampling edge.

Q257. A 4-bit Johnson counter has (Practice variation 15)

A) 4

B) 8

C) 16

D) 32

Answer: B) 8
Explanation: A Johnson counter has 2n states.

Q258. A synchronous counter uses (Practice variation 15)

A) A common clock

B) Ripple clocks only

C) No clock

D) Analog clock

Answer: A) A common clock
Explanation: All flip-flops are clocked together.

Q259. PLA has programmable (Practice variation 15)

A) AND and OR arrays

B) Only OR array

C) Only AND array

D) Only flip-flops

Answer: A) AND and OR arrays
Explanation: Both planes are programmable in a PLA.

Q260. An 8-bit ADC has (Practice variation 15)

A) 128

B) 256

C) 512

D) 1024

Answer: B) 256
Explanation: 2■ = 256 quantization levels.

Q261. The decimal value of hexadecimal F is (Practice variation 16)

A) 13

B) 14

C) 15

D) 16

Answer: C) 15
Explanation: F■■ = 15.

Q262. A + 1 equals (Practice variation 16)

A) A

B) 0

C) 1

D) A'

Answer: C) 1
Explanation: Dominance law.

Q263. A 5-variable K-map contains (Practice variation 16)

A) 8 cells

B) 16 cells

C) 32 cells

D) 64 cells

Answer: C) 32 cells
Explanation: 2■ = 32.

Q264. The sum output of a half adder uses (Practice variation 16)

A) AND

B) OR

C) XOR

D) NOR

Answer: C) XOR
Explanation: S = A XOR B.

Q265. A 16-to-1 MUX needs (Practice variation 16)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: 2■ = 16.

Q266. A T flip-flop with T=0 (Practice variation 16)

A) Holds

B) Toggles

C) Sets

D) Resets

Answer: A) Holds
Explanation: T=0 means no change.

Q267. A 16-bit register requires (Practice variation 16)

A) 8 flip-flops

B) 16 flip-flops

C) 32 flip-flops

D) 4 flip-flops

Answer: B) 16 flip-flops
Explanation: One flip-flop stores one bit.

Q268. A MOD-6 counter needs at least (Practice variation 16)

A) 2 flip-flops

B) 3 flip-flops

C) 4 flip-flops

D) 6 flip-flops

Answer: B) 3 flip-flops
Explanation: $2^3 = 8$, enough for 6 states.

Q269. SRAM is generally (Practice variation 16)

A) Faster than DRAM

B) Slower than DRAM always

C) Non-memory

D) Analog

Answer: A) Faster than DRAM
Explanation: SRAM avoids refresh and is typically faster.

Q270. CMOS is known for (Practice variation 16)

A) Low static power

B) High static power

C) No input impedance

D) No switching

Answer: A) Low static power
Explanation: CMOS draws little static power.

Q271. A binary digit is called a (Practice variation 17)

A) Byte

B) Bit

C) Nibble

D) Word

Answer: B) Bit
Explanation: A bit is one binary digit.

Q272. A · 0 equals (Practice variation 17)

A) A

B) 0

C) 1

D) A'

Answer: B) 0
Explanation: An AND with 0 is 0.

Q273. A group of 4 K-map cells eliminates (Practice variation 17)

A) 1 variable

B) 2 variables

C) 3 variables

D) 4 variables

Answer: B) 2 variables
Explanation: Each doubling of group size removes one variable.

Q274. The carry output of a half adder uses (Practice variation 17)

A) AND

B) OR

C) XOR

D) NOT

Answer: A) AND
Explanation: C = AB.

Q275. A 1-to-16 DEMUX needs (Practice variation 17)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: Four select lines choose one of 16 outputs.

Q276. A T flip-flop with T=1 (Practice variation 17)

A) Holds

B) Toggles

C) Sets only

D) Resets only

Answer: B) Toggles
Explanation: T=1 complements the state.

Q277. SIPO converts (Practice variation 17)

A) Serial to parallel

B) Parallel to serial

C) Analog to digital

D) Digital to analog

Answer: A) Serial to parallel
Explanation: SIPO expands serial data into parallel form.

Q278. A MOD-10 counter needs at least (Practice variation 17)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: 2■ = 16, enough for 10.

Q279. DRAM stores charge mainly in a (Practice variation 17)

A) Capacitor

B) Transformer

C) Relay

D) Decoder

Answer: A) Capacitor
Explanation: A DRAM cell uses a capacitor.

Q280. Fan-in means (Practice variation 17)

A) Number of gate inputs

B) Number of loads

C) Memory size

D) Clock frequency

Answer: A) Number of gate inputs
Explanation: Fan-in is input count.

Q281. The range of an unsigned 4-bit number is (Practice variation 18)

A) 0–7

B) 0–15

C) –8 to 7

D) 1–16

Answer: B) 0–15
Explanation: There are 16 values from 0 to 15.

Q282. A + A' equals (Practice variation 18)

A) A

B) 0

C) 1

D) A'

Answer: C) 1
Explanation: Complement law.

Q283. Don't-care conditions are commonly represented by (Practice variation 18)

A) X

B) Z

C) Y

D) D

Answer: A) X
Explanation: X denotes either 0 or 1 for minimization.

Q284. A full adder has (Practice variation 18)

A) 2 inputs

B) 3 inputs

C) 4 inputs

D) 5 inputs

Answer: B) 3 inputs
Explanation: A, B and Cin.

Q285. A 3-to-8 decoder has (Practice variation 18)

A) 3 outputs

B) 6 outputs

C) 8 outputs

D) 16 outputs

Answer: C) 8 outputs
Explanation: $2^3 = 8$.

Q286. A D flip-flop is commonly used in (Practice variation 18)

A) Registers

B) Transformers

C) Amplifiers

D) Filters

Answer: A) Registers
Explanation: D flip-flops form registers.

Q287. PISO converts (Practice variation 18)

A) Parallel to serial

B) Serial to parallel

C) Analog to digital

D) Digital to analog

Answer: A) Parallel to serial
Explanation: PISO shifts parallel-loaded data out serially.

Q288. A 3-bit binary counter has (Practice variation 18)

A) 4

B) 6

C) 8

D) 16

Answer: C) 8
Explanation: $2^3 = 8$ states.

Q289. EPROM is traditionally erased using (Practice variation 18)

A) UV light

B) Electrical pulse only

C) Sound

D) Magnetic field

Answer: A) UV light
Explanation: UV light erases floating-gate EPROM.

Q290. Rise time describes transition from (Practice variation 18)

A) Low to high

B) High to low

C) High to high

D) Low to low

Answer: A) Low to high
Explanation: It is the low-to-high transition time.

Q291. The range of signed 4-bit two's-complement numbers is (Practice variation 19)

A) 0–15

B) –7 to 7

C) –8 to 7

D) –15 to 15

Answer: C) –8 to 7
Explanation: The range is -2^3 to 2^3-1.

Q292. A · A' equals (Practice variation 19)

A) A

B) 0

C) 1

D) A'

Answer: B) 0
Explanation: Complement law.

Q293. Canonical SOP uses (Practice variation 19)

A) Minterms

B) Maxterms

C) Registers

D) Counters

Answer: A) Minterms
Explanation: SOP is expressed as a sum of minterms.

Q294. A comparator indicates (Practice variation 19)

A) A>B, A=B, A<B

B) Only A>B

C) Only equality

D) Only A<B

Answer: A) A>B, A=B, A<B
Explanation: A magnitude comparator gives three relations.

Q295. A 8-to-3 encoder has (Practice variation 19)

A) 8 inputs and 3 outputs

B) 3 inputs and 8 outputs

C) 8 and 8

D) 3 and 3

Answer: A) 8 inputs and 3 outputs
Explanation: It compresses one-of-eight input to 3 bits.

Q296. Setup time is the time data must be stable (Practice variation 19)

A) Before active clock edge

B) After active edge

C) Before power off

D) After reset only

Answer: A) Before active clock edge
Explanation: Setup precedes the sampling edge.

Q297. A ring counter uses (Practice variation 19)

A) Feedback

B) No feedback

C) Only analog input

D) Only a decoder

Answer: A) Feedback
Explanation: The last stage feeds the first.

Q298. A 4-bit counter divides the input frequency at its MSB by (Practice variation 19)

A) 4

B) 8

C) 16

D) 32

Answer: C) 16
Explanation: Each stage divides by 2.

Q299. FPGA stands for (Practice variation 19)

A) Field Programmable Gate Array

B) Fast Programmable Gate Array

C) Field Processing Gate Array

D) Fixed Programmable Gate Array

Answer: A) Field Programmable Gate Array
Explanation: FPGA is a programmable logic device.

Q300. Fall time describes transition from (Practice variation 19)

A) High to low

B) Low to high

C) Low to low

D) High to high

Answer: A) High to low
Explanation: It is the high-to-low transition time.

UNIT 7: Registers & Shift Registers

Q301. Which code is commonly used in shaft encoders? (Practice variation 20)

A) BCD

B) Gray

C) ASCII

D) Excess-3

Answer: B) Gray
Explanation: Gray code minimizes transition ambiguity.

Q302. Which gate is mainly used for parity checking? (Practice variation 20)

A) AND

B) OR

C) XOR

D) NOT

Answer: C) XOR
Explanation: XOR naturally detects odd parity.

Q303. Canonical POS uses (Practice variation 20)

A) Minterms

B) Maxterms

C) Flip-flops

D) Encoders

Answer: B) Maxterms
Explanation: POS is expressed as a product of maxterms.

Q304. A carry look-ahead adder is faster mainly because it (Practice variation 20)

A) Computes carry in parallel

B) Uses no gates

C) Stores carry

D) Uses analog signals

Answer: A) Computes carry in parallel
Explanation: Parallel carry computation reduces delay.

Q305. A BCD-to-7-segment circuit is a (Practice variation 20)

A) Decoder

B) Encoder

C) Adder

D) Counter

Answer: A) Decoder
Explanation: It decodes BCD into display segments.

Q306. Hold time is the time data must remain stable (Practice variation 20)

A) After active clock edge

B) Before active edge

C) Before power off

D) During reset only

Answer: A) After active clock edge
Explanation: Hold follows the sampling edge.

Q307. A 4-bit Johnson counter has (Practice variation 20)

A) 4

B) 8

C) 16

D) 32

Answer: B) 8
Explanation: A Johnson counter has 2n states.

Q308. A synchronous counter uses (Practice variation 20)

A) A common clock

B) Ripple clocks only

C) No clock

D) Analog clock

Answer: A) A common clock
Explanation: All flip-flops are clocked together.

Q309. PLA has programmable (Practice variation 20)

A) AND and OR arrays

B) Only OR array

C) Only AND array

D) Only flip-flops

Answer: A) AND and OR arrays
Explanation: Both planes are programmable in a PLA.

Q310. An 8-bit ADC has (Practice variation 20)

A) 128

B) 256

C) 512

D) 1024

Answer: B) 256
Explanation: 2■ = 256 quantization levels.

Q311. The decimal value of hexadecimal F is (Practice variation 21)

A) 13

B) 14

C) 15

D) 16

Answer: C) 15
Explanation: F■■ = 15.

Q312. A + 1 equals (Practice variation 21)

A) A

B) 0

C) 1

D) A'

Answer: C) 1
Explanation: Dominance law.

Q313. A 5-variable K-map contains (Practice variation 21)

A) 8 cells

B) 16 cells

C) 32 cells

D) 64 cells

Answer: C) 32 cells
Explanation: 2■ = 32.

Q314. The sum output of a half adder uses (Practice variation 21)

A) AND

B) OR

C) XOR

D) NOR

Answer: C) XOR
Explanation: S = A XOR B.

Q315. A 16-to-1 MUX needs (Practice variation 21)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: 2■ = 16.

Q316. A T flip-flop with T=0 (Practice variation 21)

A) Holds

B) Toggles

C) Sets

D) Resets

Answer: A) Holds
Explanation: T=0 means no change.

Q317. A 16-bit register requires (Practice variation 21)

A) 8 flip-flops

B) 16 flip-flops

C) 32 flip-flops

D) 4 flip-flops

Answer: B) 16 flip-flops
Explanation: One flip-flop stores one bit.

Q318. A MOD-6 counter needs at least (Practice variation 21)

A) 2 flip-flops

B) 3 flip-flops

C) 4 flip-flops

D) 6 flip-flops

Answer: B) 3 flip-flops
Explanation: $2^3 = 8$, enough for 6 states.

Q319. SRAM is generally (Practice variation 21)

A) Faster than DRAM

B) Slower than DRAM always

C) Non-memory

D) Analog

Answer: A) Faster than DRAM
Explanation: SRAM avoids refresh and is typically faster.

Q320. CMOS is known for (Practice variation 21)

A) Low static power

B) High static power

C) No input impedance

D) No switching

Answer: A) Low static power
Explanation: CMOS draws little static power.

Q321. A binary digit is called a (Practice variation 22)

A) Byte

B) Bit

C) Nibble

D) Word

Answer: B) Bit
Explanation: A bit is one binary digit.

Q322. A · 0 equals (Practice variation 22)

A) A

B) 0

C) 1

D) A'

Answer: B) 0
Explanation: An AND with 0 is 0.

Q323. A group of 4 K-map cells eliminates (Practice variation 22)

A) 1 variable

B) 2 variables

C) 3 variables

D) 4 variables

Answer: B) 2 variables
Explanation: Each doubling of group size removes one variable.

Q324. The carry output of a half adder uses (Practice variation 22)

A) AND

B) OR

C) XOR

D) NOT

Answer: A) AND
Explanation: C = AB.

Q325. A 1-to-16 DEMUX needs (Practice variation 22)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: Four select lines choose one of 16 outputs.

Q326. A T flip-flop with T=1 (Practice variation 22)

A) Holds

B) Toggles

C) Sets only

D) Resets only

Answer: B) Toggles
Explanation: T=1 complements the state.

Q327. SIPO converts (Practice variation 22)

A) Serial to parallel

B) Parallel to serial

C) Analog to digital

D) Digital to analog

Answer: A) Serial to parallel
Explanation: SIPO expands serial data into parallel form.

Q328. A MOD-10 counter needs at least (Practice variation 22)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: 2■ = 16, enough for 10.

Q329. DRAM stores charge mainly in a (Practice variation 22)

A) Capacitor

B) Transformer

C) Relay

D) Decoder

Answer: A) Capacitor
Explanation: A DRAM cell uses a capacitor.

Q330. Fan-in means (Practice variation 22)

A) Number of gate inputs

B) Number of loads

C) Memory size

D) Clock frequency

Answer: A) Number of gate inputs
Explanation: Fan-in is input count.

Q331. The range of an unsigned 4-bit number is (Practice variation 23)

A) 0–7

B) 0–15

C) –8 to 7

D) 1–16

Answer: B) 0–15
Explanation: There are 16 values from 0 to 15.

Q332. A + A' equals (Practice variation 23)

A) A

B) 0

C) 1

D) A'

Answer: C) 1
Explanation: Complement law.

Q333. Don't-care conditions are commonly represented by (Practice variation 23)

A) X

B) Z

C) Y

D) D

Answer: A) X
Explanation: X denotes either 0 or 1 for minimization.

Q334. A full adder has (Practice variation 23)

A) 2 inputs

B) 3 inputs

C) 4 inputs

D) 5 inputs

Answer: B) 3 inputs
Explanation: A, B and Cin.

Q335. A 3-to-8 decoder has (Practice variation 23)

A) 3 outputs

B) 6 outputs

C) 8 outputs

D) 16 outputs

Answer: C) 8 outputs
Explanation: $2^3 = 8$.

Q336. A D flip-flop is commonly used in (Practice variation 23)

A) Registers

B) Transformers

C) Amplifiers

D) Filters

Answer: A) Registers
Explanation: D flip-flops form registers.

Q337. PISO converts (Practice variation 23)

A) Parallel to serial

B) Serial to parallel

C) Analog to digital

D) Digital to analog

Answer: A) Parallel to serial
Explanation: PISO shifts parallel-loaded data out serially.

Q338. A 3-bit binary counter has (Practice variation 23)

A) 4

B) 6

C) 8

D) 16

Answer: C) 8
Explanation: $2^3 = 8$ states.

Q339. EPROM is traditionally erased using (Practice variation 23)

A) UV light

B) Electrical pulse only

C) Sound

D) Magnetic field

Answer: A) UV light
Explanation: UV light erases floating-gate EPROM.

Q340. Rise time describes transition from (Practice variation 23)

A) Low to high

B) High to low

C) High to high

D) Low to low

Answer: A) Low to high
Explanation: It is the low-to-high transition time.

Q341. The range of signed 4-bit two's-complement numbers is (Practice variation 24)

A) 0–15

B) –7 to 7

C) –8 to 7

D) –15 to 15

Answer: C) –8 to 7
Explanation: The range is -2^3 to 2^3-1.

Q342. A · A' equals (Practice variation 24)

A) A

B) 0

C) 1

D) A'

Answer: B) 0
Explanation: Complement law.

Q343. Canonical SOP uses (Practice variation 24)

A) Minterms

B) Maxterms

C) Registers

D) Counters

Answer: A) Minterms
Explanation: SOP is expressed as a sum of minterms.

Q344. A comparator indicates (Practice variation 24)

A) A>B, A=B, A<B

B) Only A>B

C) Only equality

D) Only A<B

Answer: A) A>B, A=B, A<B
Explanation: A magnitude comparator gives three relations.

Q345. A 8-to-3 encoder has (Practice variation 24)

A) 8 inputs and 3 outputs

B) 3 inputs and 8 outputs

C) 8 and 8

D) 3 and 3

Answer: A) 8 inputs and 3 outputs
Explanation: It compresses one-of-eight input to 3 bits.

Q346. Setup time is the time data must be stable (Practice variation 24)

A) Before active clock edge

B) After active edge

C) Before power off

D) After reset only

Answer: A) Before active clock edge
Explanation: Setup precedes the sampling edge.

Q347. A ring counter uses (Practice variation 24)

A) Feedback

B) No feedback

C) Only analog input

D) Only a decoder

Answer: A) Feedback
Explanation: The last stage feeds the first.

Q348. A 4-bit counter divides the input frequency at its MSB by (Practice variation 24)

A) 4

B) 8

C) 16

D) 32

Answer: C) 16
Explanation: Each stage divides by 2.

Q349. FPGA stands for (Practice variation 24)

A) Field Programmable Gate Array

B) Fast Programmable Gate Array

C) Field Processing Gate Array

D) Fixed Programmable Gate Array

Answer: A) Field Programmable Gate Array
Explanation: FPGA is a programmable logic device.

Q350. Fall time describes transition from (Practice variation 24)

A) High to low

B) Low to high

C) Low to low

D) High to high

Answer: A) High to low
Explanation: It is the high-to-low transition time.

UNIT 8: Counters

Q351. Which code is commonly used in shaft encoders? (Practice variation 25)

A) BCD

B) Gray

C) ASCII

D) Excess-3

Answer: B) Gray
Explanation: Gray code minimizes transition ambiguity.

Q352. Which gate is mainly used for parity checking? (Practice variation 25)

A) AND

B) OR

C) XOR

D) NOT

Answer: C) XOR
Explanation: XOR naturally detects odd parity.

Q353. Canonical POS uses (Practice variation 25)

A) Minterms

B) Maxterms

C) Flip-flops

D) Encoders

Answer: B) Maxterms
Explanation: POS is expressed as a product of maxterms.

Q354. A carry look-ahead adder is faster mainly because it (Practice variation 25)

A) Computes carry in parallel

B) Uses no gates

C) Stores carry

D) Uses analog signals

Answer: A) Computes carry in parallel
Explanation: Parallel carry computation reduces delay.

Q355. A BCD-to-7-segment circuit is a (Practice variation 25)

A) Decoder

B) Encoder

C) Adder

D) Counter

Answer: A) Decoder
Explanation: It decodes BCD into display segments.

Q356. Hold time is the time data must remain stable (Practice variation 25)

A) After active clock edge

B) Before active edge

C) Before power off

D) During reset only

Answer: A) After active clock edge
Explanation: Hold follows the sampling edge.

Q357. A 4-bit Johnson counter has (Practice variation 25)

A) 4

B) 8

C) 16

D) 32

Answer: B) 8
Explanation: A Johnson counter has 2n states.

Q358. A synchronous counter uses (Practice variation 25)

A) A common clock

B) Ripple clocks only

C) No clock

D) Analog clock

Answer: A) A common clock
Explanation: All flip-flops are clocked together.

Q359. PLA has programmable (Practice variation 25)

A) AND and OR arrays

B) Only OR array

C) Only AND array

D) Only flip-flops

Answer: A) AND and OR arrays
Explanation: Both planes are programmable in a PLA.

Q360. An 8-bit ADC has (Practice variation 25)

A) 128

B) 256

C) 512

D) 1024

Answer: B) 256
Explanation: 2■ = 256 quantization levels.

Q361. The decimal value of hexadecimal F is (Practice variation 26)

A) 13

B) 14

C) 15

D) 16

Answer: C) 15
Explanation: F■■ = 15.

Q362. A + 1 equals (Practice variation 26)

A) A

B) 0

C) 1

D) A'

Answer: C) 1
Explanation: Dominance law.

Q363. A 5-variable K-map contains (Practice variation 26)

A) 8 cells

B) 16 cells

C) 32 cells

D) 64 cells

Answer: C) 32 cells
Explanation: 2■ = 32.

Q364. The sum output of a half adder uses (Practice variation 26)

A) AND

B) OR

C) XOR

D) NOR

Answer: C) XOR
Explanation: S = A XOR B.

Q365. A 16-to-1 MUX needs (Practice variation 26)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: 2■ = 16.

Q366. A T flip-flop with T=0 (Practice variation 26)

A) Holds

B) Toggles

C) Sets

D) Resets

Answer: A) Holds
Explanation: T=0 means no change.

Q367. A 16-bit register requires (Practice variation 26)

A) 8 flip-flops

B) 16 flip-flops

C) 32 flip-flops

D) 4 flip-flops

Answer: B) 16 flip-flops
Explanation: One flip-flop stores one bit.

Q368. A MOD-6 counter needs at least (Practice variation 26)

A) 2 flip-flops

B) 3 flip-flops

C) 4 flip-flops

D) 6 flip-flops

Answer: B) 3 flip-flops
Explanation: $2^3 = 8$, enough for 6 states.

Q369. SRAM is generally (Practice variation 26)

A) Faster than DRAM

B) Slower than DRAM always

C) Non-memory

D) Analog

Answer: A) Faster than DRAM
Explanation: SRAM avoids refresh and is typically faster.

Q370. CMOS is known for (Practice variation 26)

A) Low static power

B) High static power

C) No input impedance

D) No switching

Answer: A) Low static power
Explanation: CMOS draws little static power.

Q371. A binary digit is called a (Practice variation 27)

A) Byte

B) Bit

C) Nibble

D) Word

Answer: B) Bit
Explanation: A bit is one binary digit.

Q372. A · 0 equals (Practice variation 27)

A) A

B) 0

C) 1

D) A'

Answer: B) 0
Explanation: An AND with 0 is 0.

Q373. A group of 4 K-map cells eliminates (Practice variation 27)

A) 1 variable

B) 2 variables

C) 3 variables

D) 4 variables

Answer: B) 2 variables
Explanation: Each doubling of group size removes one variable.

Q374. The carry output of a half adder uses (Practice variation 27)

A) AND

B) OR

C) XOR

D) NOT

Answer: A) AND
Explanation: C = AB.

Q375. A 1-to-16 DEMUX needs (Practice variation 27)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: Four select lines choose one of 16 outputs.

Q376. A T flip-flop with T=1 (Practice variation 27)

A) Holds

B) Toggles

C) Sets only

D) Resets only

Answer: B) Toggles
Explanation: T=1 complements the state.

Q377. SIPO converts (Practice variation 27)

A) Serial to parallel

B) Parallel to serial

C) Analog to digital

D) Digital to analog

Answer: A) Serial to parallel
Explanation: SIPO expands serial data into parallel form.

Q378. A MOD-10 counter needs at least (Practice variation 27)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: 2■ = 16, enough for 10.

Q379. DRAM stores charge mainly in a (Practice variation 27)

A) Capacitor

B) Transformer

C) Relay

D) Decoder

Answer: A) Capacitor
Explanation: A DRAM cell uses a capacitor.

Q380. Fan-in means (Practice variation 27)

A) Number of gate inputs

B) Number of loads

C) Memory size

D) Clock frequency

Answer: A) Number of gate inputs
Explanation: Fan-in is input count.

Q381. The range of an unsigned 4-bit number is (Practice variation 28)

A) 0–7

B) 0–15

C) –8 to 7

D) 1–16

Answer: B) 0–15
Explanation: There are 16 values from 0 to 15.

Q382. A + A' equals (Practice variation 28)

A) A

B) 0

C) 1

D) A'

Answer: C) 1
Explanation: Complement law.

Q383. Don't-care conditions are commonly represented by (Practice variation 28)

A) X

B) Z

C) Y

D) D

Answer: A) X
Explanation: X denotes either 0 or 1 for minimization.

Q384. A full adder has (Practice variation 28)

A) 2 inputs

B) 3 inputs

C) 4 inputs

D) 5 inputs

Answer: B) 3 inputs
Explanation: A, B and Cin.

Q385. A 3-to-8 decoder has (Practice variation 28)

A) 3 outputs

B) 6 outputs

C) 8 outputs

D) 16 outputs

Answer: C) 8 outputs
Explanation: $2^3 = 8$.

Q386. A D flip-flop is commonly used in (Practice variation 28)

A) Registers

B) Transformers

C) Amplifiers

D) Filters

Answer: A) Registers
Explanation: D flip-flops form registers.

Q387. PISO converts (Practice variation 28)

A) Parallel to serial

B) Serial to parallel

C) Analog to digital

D) Digital to analog

Answer: A) Parallel to serial
Explanation: PISO shifts parallel-loaded data out serially.

Q388. A 3-bit binary counter has (Practice variation 28)

A) 4

B) 6

C) 8

D) 16

Answer: C) 8
Explanation: $2^3 = 8$ states.

Q389. EPROM is traditionally erased using (Practice variation 28)

A) UV light

B) Electrical pulse only

C) Sound

D) Magnetic field

Answer: A) UV light
Explanation: UV light erases floating-gate EPROM.

Q390. Rise time describes transition from (Practice variation 28)

A) Low to high

B) High to low

C) High to high

D) Low to low

Answer: A) Low to high
Explanation: It is the low-to-high transition time.

Q391. The range of signed 4-bit two's-complement numbers is (Practice variation 29)

A) 0–15

B) –7 to 7

C) –8 to 7

D) –15 to 15

Answer: C) –8 to 7
Explanation: The range is -2^3 to 2^3-1.

Q392. A · A' equals (Practice variation 29)

A) A

B) 0

C) 1

D) A'

Answer: B) 0
Explanation: Complement law.

Q393. Canonical SOP uses (Practice variation 29)

A) Minterms

B) Maxterms

C) Registers

D) Counters

Answer: A) Minterms
Explanation: SOP is expressed as a sum of minterms.

Q394. A comparator indicates (Practice variation 29)

A) A>B, A=B, A<B

B) Only A>B

C) Only equality

D) Only A<B

Answer: A) A>B, A=B, A<B
Explanation: A magnitude comparator gives three relations.

Q395. A 8-to-3 encoder has (Practice variation 29)

A) 8 inputs and 3 outputs

B) 3 inputs and 8 outputs

C) 8 and 8

D) 3 and 3

Answer: A) 8 inputs and 3 outputs
Explanation: It compresses one-of-eight input to 3 bits.

Q396. Setup time is the time data must be stable (Practice variation 29)

A) Before active clock edge

B) After active edge

C) Before power off

D) After reset only

Answer: A) Before active clock edge
Explanation: Setup precedes the sampling edge.

Q397. A ring counter uses (Practice variation 29)

A) Feedback

B) No feedback

C) Only analog input

D) Only a decoder

Answer: A) Feedback
Explanation: The last stage feeds the first.

Q398. A 4-bit counter divides the input frequency at its MSB by (Practice variation 29)

A) 4

B) 8

C) 16

D) 32

Answer: C) 16
Explanation: Each stage divides by 2.

Q399. FPGA stands for (Practice variation 29)

A) Field Programmable Gate Array

B) Fast Programmable Gate Array

C) Field Processing Gate Array

D) Fixed Programmable Gate Array

Answer: A) Field Programmable Gate Array
Explanation: FPGA is a programmable logic device.

Q400. Fall time describes transition from (Practice variation 29)

A) High to low

B) Low to high

C) Low to low

D) High to high

Answer: A) High to low
Explanation: It is the high-to-low transition time.

UNIT 9: Memory & Programmable Logic

Q401. Which code is commonly used in shaft encoders? (Practice variation 30)

A) BCD

B) Gray

C) ASCII

D) Excess-3

Answer: B) Gray
Explanation: Gray code minimizes transition ambiguity.

Q402. Which gate is mainly used for parity checking? (Practice variation 30)

A) AND

B) OR

C) XOR

D) NOT

Answer: C) XOR
Explanation: XOR naturally detects odd parity.

Q403. Canonical POS uses (Practice variation 30)

A) Minterms

B) Maxterms

C) Flip-flops

D) Encoders

Answer: B) Maxterms
Explanation: POS is expressed as a product of maxterms.

Q404. A carry look-ahead adder is faster mainly because it (Practice variation 30)

A) Computes carry in parallel

B) Uses no gates

C) Stores carry

D) Uses analog signals

Answer: A) Computes carry in parallel
Explanation: Parallel carry computation reduces delay.

Q405. A BCD-to-7-segment circuit is a (Practice variation 30)

A) Decoder

B) Encoder

C) Adder

D) Counter

Answer: A) Decoder
Explanation: It decodes BCD into display segments.

Q406. Hold time is the time data must remain stable (Practice variation 30)

A) After active clock edge

B) Before active edge

C) Before power off

D) During reset only

Answer: A) After active clock edge
Explanation: Hold follows the sampling edge.

Q407. A 4-bit Johnson counter has (Practice variation 30)

A) 4

B) 8

C) 16

D) 32

Answer: B) 8
Explanation: A Johnson counter has 2n states.

Q408. A synchronous counter uses (Practice variation 30)

A) A common clock

B) Ripple clocks only

C) No clock

D) Analog clock

Answer: A) A common clock
Explanation: All flip-flops are clocked together.

Q409. PLA has programmable (Practice variation 30)

A) AND and OR arrays

B) Only OR array

C) Only AND array

D) Only flip-flops

Answer: A) AND and OR arrays
Explanation: Both planes are programmable in a PLA.

Q410. An 8-bit ADC has (Practice variation 30)

A) 128

B) 256

C) 512

D) 1024

Answer: B) 256
Explanation: 2■ = 256 quantization levels.

Q411. The decimal value of hexadecimal F is (Practice variation 31)

A) 13

B) 14

C) 15

D) 16

Answer: C) 15
Explanation: F■■ = 15.

Q412. A + 1 equals (Practice variation 31)

A) A

B) 0

C) 1

D) A'

Answer: C) 1
Explanation: Dominance law.

Q413. A 5-variable K-map contains (Practice variation 31)

A) 8 cells

B) 16 cells

C) 32 cells

D) 64 cells

Answer: C) 32 cells
Explanation: 2■ = 32.

Q414. The sum output of a half adder uses (Practice variation 31)

A) AND

B) OR

C) XOR

D) NOR

Answer: C) XOR
Explanation: S = A XOR B.

Q415. A 16-to-1 MUX needs (Practice variation 31)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: 2■ = 16.

Q416. A T flip-flop with T=0 (Practice variation 31)

A) Holds

B) Toggles

C) Sets

D) Resets

Answer: A) Holds
Explanation: T=0 means no change.

Q417. A 16-bit register requires (Practice variation 31)

A) 8 flip-flops

B) 16 flip-flops

C) 32 flip-flops

D) 4 flip-flops

Answer: B) 16 flip-flops
Explanation: One flip-flop stores one bit.

Q418. A MOD-6 counter needs at least (Practice variation 31)

A) 2 flip-flops

B) 3 flip-flops

C) 4 flip-flops

D) 6 flip-flops

Answer: B) 3 flip-flops
Explanation: $2^3 = 8$, enough for 6 states.

Q419. SRAM is generally (Practice variation 31)

A) Faster than DRAM

B) Slower than DRAM always

C) Non-memory

D) Analog

Answer: A) Faster than DRAM
Explanation: SRAM avoids refresh and is typically faster.

Q420. CMOS is known for (Practice variation 31)

A) Low static power

B) High static power

C) No input impedance

D) No switching

Answer: A) Low static power
Explanation: CMOS draws little static power.

Q421. A binary digit is called a (Practice variation 32)

A) Byte

B) Bit

C) Nibble

D) Word

Answer: B) Bit
Explanation: A bit is one binary digit.

Q422. A · 0 equals (Practice variation 32)

A) A

B) 0

C) 1

D) A'

Answer: B) 0
Explanation: An AND with 0 is 0.

Q423. A group of 4 K-map cells eliminates (Practice variation 32)

A) 1 variable

B) 2 variables

C) 3 variables

D) 4 variables

Answer: B) 2 variables
Explanation: Each doubling of group size removes one variable.

Q424. The carry output of a half adder uses (Practice variation 32)

A) AND

B) OR

C) XOR

D) NOT

Answer: A) AND
Explanation: C = AB.

Q425. A 1-to-16 DEMUX needs (Practice variation 32)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: Four select lines choose one of 16 outputs.

Q426. A T flip-flop with T=1 (Practice variation 32)

A) Holds

B) Toggles

C) Sets only

D) Resets only

Answer: B) Toggles
Explanation: T=1 complements the state.

Q427. SIPO converts (Practice variation 32)

A) Serial to parallel

B) Parallel to serial

C) Analog to digital

D) Digital to analog

Answer: A) Serial to parallel
Explanation: SIPO expands serial data into parallel form.

Q428. A MOD-10 counter needs at least (Practice variation 32)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: 2■ = 16, enough for 10.

Q429. DRAM stores charge mainly in a (Practice variation 32)

A) Capacitor

B) Transformer

C) Relay

D) Decoder

Answer: A) Capacitor
Explanation: A DRAM cell uses a capacitor.

Q430. Fan-in means (Practice variation 32)

A) Number of gate inputs

B) Number of loads

C) Memory size

D) Clock frequency

Answer: A) Number of gate inputs
Explanation: Fan-in is input count.

Q431. The range of an unsigned 4-bit number is (Practice variation 33)

A) 0–7

B) 0–15

C) –8 to 7

D) 1–16

Answer: B) 0–15
Explanation: There are 16 values from 0 to 15.

Q432. A + A' equals (Practice variation 33)

A) A

B) 0

C) 1

D) A'

Answer: C) 1
Explanation: Complement law.

Q433. Don't-care conditions are commonly represented by (Practice variation 33)

A) X

B) Z

C) Y

D) D

Answer: A) X
Explanation: X denotes either 0 or 1 for minimization.

Q434. A full adder has (Practice variation 33)

A) 2 inputs

B) 3 inputs

C) 4 inputs

D) 5 inputs

Answer: B) 3 inputs
Explanation: A, B and Cin.

Q435. A 3-to-8 decoder has (Practice variation 33)

A) 3 outputs

B) 6 outputs

C) 8 outputs

D) 16 outputs

Answer: C) 8 outputs
Explanation: $2^3 = 8$.

Q436. A D flip-flop is commonly used in (Practice variation 33)

A) Registers

B) Transformers

C) Amplifiers

D) Filters

Answer: A) Registers
Explanation: D flip-flops form registers.

Q437. PISO converts (Practice variation 33)

A) Parallel to serial

B) Serial to parallel

C) Analog to digital

D) Digital to analog

Answer: A) Parallel to serial
Explanation: PISO shifts parallel-loaded data out serially.

Q438. A 3-bit binary counter has (Practice variation 33)

A) 4

B) 6

C) 8

D) 16

Answer: C) 8
Explanation: $2^3 = 8$ states.

Q439. EPROM is traditionally erased using (Practice variation 33)

A) UV light

B) Electrical pulse only

C) Sound

D) Magnetic field

Answer: A) UV light
Explanation: UV light erases floating-gate EPROM.

Q440. Rise time describes transition from (Practice variation 33)

A) Low to high

B) High to low

C) High to high

D) Low to low

Answer: A) Low to high
Explanation: It is the low-to-high transition time.

Q441. The range of signed 4-bit two's-complement numbers is (Practice variation 34)

A) 0–15

B) –7 to 7

C) –8 to 7

D) –15 to 15

Answer: C) –8 to 7
Explanation: The range is -2^3 to 2^3-1.

Q442. A · A' equals (Practice variation 34)

A) A

B) 0

C) 1

D) A'

Answer: B) 0
Explanation: Complement law.

Q443. Canonical SOP uses (Practice variation 34)

A) Minterms

B) Maxterms

C) Registers

D) Counters

Answer: A) Minterms
Explanation: SOP is expressed as a sum of minterms.

Q444. A comparator indicates (Practice variation 34)

A) A>B, A=B, A<B

B) Only A>B

C) Only equality

D) Only A<B

Answer: A) A>B, A=B, A<B
Explanation: A magnitude comparator gives three relations.

Q445. A 8-to-3 encoder has (Practice variation 34)

A) 8 inputs and 3 outputs

B) 3 inputs and 8 outputs

C) 8 and 8

D) 3 and 3

Answer: A) 8 inputs and 3 outputs
Explanation: It compresses one-of-eight input to 3 bits.

Q446. Setup time is the time data must be stable (Practice variation 34)

A) Before active clock edge

B) After active edge

C) Before power off

D) After reset only

Answer: A) Before active clock edge
Explanation: Setup precedes the sampling edge.

Q447. A ring counter uses (Practice variation 34)

A) Feedback

B) No feedback

C) Only analog input

D) Only a decoder

Answer: A) Feedback
Explanation: The last stage feeds the first.

Q448. A 4-bit counter divides the input frequency at its MSB by (Practice variation 34)

A) 4

B) 8

C) 16

D) 32

Answer: C) 16
Explanation: Each stage divides by 2.

Q449. FPGA stands for (Practice variation 34)

A) Field Programmable Gate Array

B) Fast Programmable Gate Array

C) Field Processing Gate Array

D) Fixed Programmable Gate Array

Answer: A) Field Programmable Gate Array
Explanation: FPGA is a programmable logic device.

Q450. Fall time describes transition from (Practice variation 34)

A) High to low

B) Low to high

C) Low to low

D) High to high

Answer: A) High to low
Explanation: It is the high-to-low transition time.

UNIT 10: Digital Logic Families & Mixed Topics

Q451. Which code is commonly used in shaft encoders? (Practice variation 35)

A) BCD

B) Gray

C) ASCII

D) Excess-3

Answer: B) Gray
Explanation: Gray code minimizes transition ambiguity.

Q452. Which gate is mainly used for parity checking? (Practice variation 35)

A) AND

B) OR

C) XOR

D) NOT

Answer: C) XOR
Explanation: XOR naturally detects odd parity.

Q453. Canonical POS uses (Practice variation 35)

A) Minterms

B) Maxterms

C) Flip-flops

D) Encoders

Answer: B) Maxterms
Explanation: POS is expressed as a product of maxterms.

Q454. A carry look-ahead adder is faster mainly because it (Practice variation 35)

A) Computes carry in parallel

B) Uses no gates

C) Stores carry

D) Uses analog signals

Answer: A) Computes carry in parallel
Explanation: Parallel carry computation reduces delay.

Q455. A BCD-to-7-segment circuit is a (Practice variation 35)

A) Decoder

B) Encoder

C) Adder

D) Counter

Answer: A) Decoder
Explanation: It decodes BCD into display segments.

Q456. Hold time is the time data must remain stable (Practice variation 35)

A) After active clock edge

B) Before active edge

C) Before power off

D) During reset only

Answer: A) After active clock edge
Explanation: Hold follows the sampling edge.

Q457. A 4-bit Johnson counter has (Practice variation 35)

A) 4

B) 8

C) 16

D) 32

Answer: B) 8
Explanation: A Johnson counter has 2n states.

Q458. A synchronous counter uses (Practice variation 35)

A) A common clock

B) Ripple clocks only

C) No clock

D) Analog clock

Answer: A) A common clock
Explanation: All flip-flops are clocked together.

Q459. PLA has programmable (Practice variation 35)

A) AND and OR arrays

B) Only OR array

C) Only AND array

D) Only flip-flops

Answer: A) AND and OR arrays
Explanation: Both planes are programmable in a PLA.

Q460. An 8-bit ADC has (Practice variation 35)

A) 128

B) 256

C) 512

D) 1024

Answer: B) 256
Explanation: 2■ = 256 quantization levels.

Q461. The decimal value of hexadecimal F is (Practice variation 36)

A) 13

B) 14

C) 15

D) 16

Answer: C) 15
Explanation: F■■ = 15.

Q462. A + 1 equals (Practice variation 36)

A) A

B) 0

C) 1

D) A'

Answer: C) 1
Explanation: Dominance law.

Q463. A 5-variable K-map contains (Practice variation 36)

A) 8 cells

B) 16 cells

C) 32 cells

D) 64 cells

Answer: C) 32 cells
Explanation: 2■ = 32.

Q464. The sum output of a half adder uses (Practice variation 36)

A) AND

B) OR

C) XOR

D) NOR

Answer: C) XOR
Explanation: S = A XOR B.

Q465. A 16-to-1 MUX needs (Practice variation 36)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: 2■ = 16.

Q466. A T flip-flop with T=0 (Practice variation 36)

A) Holds

B) Toggles

C) Sets

D) Resets

Answer: A) Holds
Explanation: T=0 means no change.

Q467. A 16-bit register requires (Practice variation 36)

A) 8 flip-flops

B) 16 flip-flops

C) 32 flip-flops

D) 4 flip-flops

Answer: B) 16 flip-flops
Explanation: One flip-flop stores one bit.

Q468. A MOD-6 counter needs at least (Practice variation 36)

A) 2 flip-flops

B) 3 flip-flops

C) 4 flip-flops

D) 6 flip-flops

Answer: B) 3 flip-flops
Explanation: $2^3 = 8$, enough for 6 states.

Q469. SRAM is generally (Practice variation 36)

A) Faster than DRAM

B) Slower than DRAM always

C) Non-memory

D) Analog

Answer: A) Faster than DRAM
Explanation: SRAM avoids refresh and is typically faster.

Q470. CMOS is known for (Practice variation 36)

A) Low static power

B) High static power

C) No input impedance

D) No switching

Answer: A) Low static power
Explanation: CMOS draws little static power.

Q471. A binary digit is called a (Practice variation 37)

A) Byte

B) Bit

C) Nibble

D) Word

Answer: B) Bit
Explanation: A bit is one binary digit.

Q472. A · 0 equals (Practice variation 37)

A) A

B) 0

C) 1

D) A'

Answer: B) 0
Explanation: An AND with 0 is 0.

Q473. A group of 4 K-map cells eliminates (Practice variation 37)

A) 1 variable

B) 2 variables

C) 3 variables

D) 4 variables

Answer: B) 2 variables
Explanation: Each doubling of group size removes one variable.

Q474. The carry output of a half adder uses (Practice variation 37)

A) AND

B) OR

C) XOR

D) NOT

Answer: A) AND
Explanation: C = AB.

Q475. A 1-to-16 DEMUX needs (Practice variation 37)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: Four select lines choose one of 16 outputs.

Q476. A T flip-flop with T=1 (Practice variation 37)

A) Holds

B) Toggles

C) Sets only

D) Resets only

Answer: B) Toggles
Explanation: T=1 complements the state.

Q477. SIPO converts (Practice variation 37)

A) Serial to parallel

B) Parallel to serial

C) Analog to digital

D) Digital to analog

Answer: A) Serial to parallel
Explanation: SIPO expands serial data into parallel form.

Q478. A MOD-10 counter needs at least (Practice variation 37)

A) 2

B) 3

C) 4

D) 5

Answer: C) 4
Explanation: 2■ = 16, enough for 10.

Q479. DRAM stores charge mainly in a (Practice variation 37)

A) Capacitor

B) Transformer

C) Relay

D) Decoder

Answer: A) Capacitor
Explanation: A DRAM cell uses a capacitor.

Q480. Fan-in means (Practice variation 37)

A) Number of gate inputs

B) Number of loads

C) Memory size

D) Clock frequency

Answer: A) Number of gate inputs
Explanation: Fan-in is input count.

Q481. The range of an unsigned 4-bit number is (Practice variation 38)

A) 0–7

B) 0–15

C) –8 to 7

D) 1–16

Answer: B) 0–15
Explanation: There are 16 values from 0 to 15.

Q482. A + A' equals (Practice variation 38)

A) A

B) 0

C) 1

D) A'

Answer: C) 1
Explanation: Complement law.

Q483. Don't-care conditions are commonly represented by (Practice variation 38)

A) X

B) Z

C) Y

D) D

Answer: A) X
Explanation: X denotes either 0 or 1 for minimization.

Q484. A full adder has (Practice variation 38)

A) 2 inputs

B) 3 inputs

C) 4 inputs

D) 5 inputs

Answer: B) 3 inputs
Explanation: A, B and Cin.

Q485. A 3-to-8 decoder has (Practice variation 38)

A) 3 outputs

B) 6 outputs

C) 8 outputs

D) 16 outputs

Answer: C) 8 outputs
Explanation: $2^3 = 8$.

Q486. A D flip-flop is commonly used in (Practice variation 38)

A) Registers

B) Transformers

C) Amplifiers

D) Filters

Answer: A) Registers
Explanation: D flip-flops form registers.

Q487. PISO converts (Practice variation 38)

A) Parallel to serial

B) Serial to parallel

C) Analog to digital

D) Digital to analog

Answer: A) Parallel to serial
Explanation: PISO shifts parallel-loaded data out serially.

Q488. A 3-bit binary counter has (Practice variation 38)

A) 4

B) 6

C) 8

D) 16

Answer: C) 8
Explanation: $2^3 = 8$ states.

Q489. EPROM is traditionally erased using (Practice variation 38)

A) UV light

B) Electrical pulse only

C) Sound

D) Magnetic field

Answer: A) UV light
Explanation: UV light erases floating-gate EPROM.

Q490. Rise time describes transition from (Practice variation 38)

A) Low to high

B) High to low

C) High to high

D) Low to low

Answer: A) Low to high
Explanation: It is the low-to-high transition time.

Q491. The range of signed 4-bit two's-complement numbers is (Practice variation 39)

A) 0–15

B) –7 to 7

C) –8 to 7

D) –15 to 15

Answer: C) –8 to 7
Explanation: The range is -2^3 to 2^3-1.

Q492. A · A' equals (Practice variation 39)

A) A

B) 0

C) 1

D) A'

Answer: B) 0
Explanation: Complement law.

Q493. Canonical SOP uses (Practice variation 39)

A) Minterms

B) Maxterms

C) Registers

D) Counters

Answer: A) Minterms
Explanation: SOP is expressed as a sum of minterms.

Q494. A comparator indicates (Practice variation 39)

A) A>B, A=B, A<B

B) Only A>B

C) Only equality

D) Only A<B

Answer: A) A>B, A=B, A<B
Explanation: A magnitude comparator gives three relations.

Q495. A 8-to-3 encoder has (Practice variation 39)

A) 8 inputs and 3 outputs

B) 3 inputs and 8 outputs

C) 8 and 8

D) 3 and 3

Answer: A) 8 inputs and 3 outputs
Explanation: It compresses one-of-eight input to 3 bits.

Q496. Setup time is the time data must be stable (Practice variation 39)

A) Before active clock edge

B) After active edge

C) Before power off

D) After reset only

Answer: A) Before active clock edge
Explanation: Setup precedes the sampling edge.

Q497. A ring counter uses (Practice variation 39)

A) Feedback

B) No feedback

C) Only analog input

D) Only a decoder

Answer: A) Feedback
Explanation: The last stage feeds the first.

Q498. A 4-bit counter divides the input frequency at its MSB by (Practice variation 39)

A) 4

B) 8

C) 16

D) 32

Answer: C) 16
Explanation: Each stage divides by 2.

Q499. FPGA stands for (Practice variation 39)

A) Field Programmable Gate Array

B) Fast Programmable Gate Array

C) Field Processing Gate Array

D) Fixed Programmable Gate Array

Answer: A) Field Programmable Gate Array
Explanation: FPGA is a programmable logic device.

Q500. Fall time describes transition from (Practice variation 39)

A) High to low

B) Low to high

C) Low to low

D) High to high

Answer: A) High to low
Explanation: It is the high-to-low transition time.