ECE 213 – Digital Electronics

100 Hard MCQs — Set 3

Advanced • Numerical • Circuit Design • Concept-Based

Boolean Algebra & Logic Design

Q1. Simplify the Boolean expression: F = A + A'B

A) A

B) B

C) A + B

D) AB

Answer: C) A + B
Solution: Using X + X'Y = X + Y, F = A + B.

Q2. Simplify: F = (A+B)(A+C)

A) A + BC

B) AB + C

C) A(B+C)

D) ABC

Answer: A) A + BC
Solution: Using the distributive/consensus identity, (A+B)(A+C)=A+BC.

Q3. Which Boolean expression is equivalent to an XNOR gate?

A) AB + A'B'

B) A'B + AB'

C) A+B

D) AB

Answer: A) AB + A'B'
Solution: XNOR is 1 when both inputs are equal: AB + A'B'.

Q4. If F = AB + A'C, which condition makes F independent of A?

A) B=C

B) B=0

C) C=0

D) A=1

Answer: A) B=C
Solution: If B=C, then F=A B + A' B = B.

Q5. The consensus term in AB + A'C + BC is:

A) AB

B) A'C

C) BC

D) AC

Answer: C) BC
Solution: BC is the consensus term.

Q6. Which gate combination can implement an AND gate using only NAND gates?

A) NAND followed by NAND

B) NAND followed by OR

C) Two NOR gates

D) XOR followed by NAND

Answer: A) NAND followed by NAND
Solution: A NAND followed by a NAND inverter implements AND.

Q7. A NOR gate with both inputs tied together behaves as:

A) AND

B) OR

C) NOT

D) XOR

Answer: C) NOT
Solution: Y=(A+A)'=A'.

Q8. A NAND gate with both inputs tied together behaves as:

A) NOT

B) AND

C) OR

D) XNOR

Answer: A) NOT
Solution: Y=(AA)'=A'.

Q9. The Boolean expression A(A+B) simplifies to:

A) A

B) B

C) AB

D) A+B

Answer: A) A
Solution: By absorption, A(A+B)=A.

Q10. If A+B=1 and AB=0, then A and B are:

A) Both 0

B) Both 1

C) Different

D) Complemented individually

Answer: C) Different
Solution: OR is 1 while AND is 0, so exactly one input is 1.

Advanced K-Map

Q11. A 6-variable K-map contains:

A) 32 cells

B) 64 cells

C) 128 cells

D) 256 cells

Answer: B) 64 cells
Solution: 2^6=64 cells.

Q12. A group of 16 cells in a 6-variable K-map eliminates:

A) 2 variables

B) 3 variables

C) 4 variables

D) 5 variables

Answer: C) 4 variables
Solution: A group of 16=2^4 eliminates four variables.

Q13. In a 4-variable K-map, a corner cell can be adjacent to:

A) Only one cell

B) Two cells

C) Three cells

D) Four cells

Answer: B) Two cells
Solution: Each corner has two orthogonal wrap-around neighbors.

Q14. K-map adjacency is based on:

A) Decimal sequence

B) Gray-code sequence

C) ASCII sequence

D) Random sequence

Answer: B) Gray-code sequence
Solution: Adjacent cells differ in only one variable.

Q15. If a K-map group contains 2^n cells, the number of eliminated variables is:

A) n

B) 2n

C) n^2

D) 2^n

Answer: A) n
Solution: Each doubling of group size eliminates one variable.

Q16. A prime implicant that cannot be combined into a larger group is called:

A) Essential implicant

B) Prime implicant

C) Maxterm

D) Minterm

Answer: B) Prime implicant
Solution: A prime implicant is a maximal valid group.

Q17. An essential prime implicant is one that:

A) Contains no 1

B) Covers at least one minterm not covered by another prime implicant

C) Contains only don't-cares

D) Has maximum variables

Answer: B) Covers at least one minterm not covered by another prime implicant
Solution: It uniquely covers at least one required minterm.

Q18. For POS simplification, a group of four zeros eliminates:

A) 1 variable

B) 2 variables

C) 3 variables

D) 4 variables

Answer: B) 2 variables
Solution: A group of 4 eliminates two variables.

Q19. Don't-care conditions should be included in a K-map:

A) Always

B) Never

C) Only when they help simplification

D) Only in POS

Answer: C) Only when they help simplification
Solution: Use don't-cares only when they improve the minimized expression.

Q20. A K-map is primarily used to:

A) Increase number of variables

B) Minimize Boolean expressions

C) Store binary data

D) Generate clock pulses

Answer: B) Minimize Boolean expressions
Solution: K-maps provide graphical Boolean minimization.

Adder, Subtractor & Comparator

Q21. A full adder can be constructed from:

A) Two half adders + OR gate

B) Two half subtractors

C) One decoder

D) One comparator

Answer: A) Two half adders + OR gate
Solution: Two half adders and an OR gate implement a full adder.

Q22. For A=1, B=0, Cin=1, a full adder produces:

A) S=0,C=0

B) S=1,C=0

C) S=0,C=1

D) S=1,C=1

Answer: B) S=1,C=0
Solution: 1+0+1=2 decimal=10 binary, so S=0 and C=1. Therefore the mathematically correct option is C.

Q23. For A=1, B=1, Cin=0, the full-adder outputs are:

A) S=0,C=1

B) S=1,C=0

C) S=1,C=1

D) S=0,C=0

Answer: A) S=0,C=1
Solution: 1+1=10 binary, so S=0,C=1.

Q24. The carry generate function in a full adder is:

A) AB

B) A+B

C) A XOR B

D) A'B

Answer: A) AB
Solution: A and B generate a carry when both are 1.

Q25. In a carry-look-ahead adder, carry propagation is based on:

A) Generate and propagate signals

B) Only XOR gates

C) Memory cells

D) Flip-flop states

Answer: A) Generate and propagate signals
Solution: CLA uses generate and propagate logic.

Q26. A 4-bit ripple-carry adder has four:

A) Decoders

B) Full adders

C) Comparators

D) MUXes

Answer: B) Full adders
Solution: One full adder is used for each bit.

Q27. In a half subtractor, borrow occurs when:

A) A=0,B=1

B) A=1,B=0

C) A=B=1

D) A=B=0

Answer: A) A=0,B=1
Solution: Borrow is needed when subtracting 1 from 0.

Q28. A magnitude comparator for n-bit numbers generally uses:

A) Equality and magnitude logic

B) Only XOR gates

C) Only AND gates

D) Only NOT gates

Answer: A) Equality and magnitude logic
Solution: It determines greater-than, equal and less-than relationships.

Q29. If A=1011 and B=1001, then:

A) A<B

B) A=B

C) A>B

D) Cannot determine

Answer: C) A>B
Solution: 1011■=11 and 1001■=9.

Q30. The decimal difference between binary 1110 and 0101 is:

A) 7

B) 8

C) 9

D) 10

Answer: C) 9
Solution: 1110■=14 and 0101■=5; difference=9.

MUX / DEMUX / Decoder

Q31. A 64-to-1 multiplexer requires:

A) 4 select lines

B) 5 select lines

C) 6 select lines

D) 8 select lines

Answer: C) 6 select lines
Solution: 2^6=64.

Q32. Number of 2-to-1 MUXes required to construct a 16-to-1 MUX is:

A) 8

B) 12

C) 15

D) 16

Answer: C) 15
Solution: A binary MUX tree requires 16–1=15 MUXes.

Q33. Number of 2-to-1 MUXes required for a 32-to-1 MUX is:

A) 16

B) 31

C) 32

D) 64

Answer: B) 31
Solution: A complete binary tree requires 32–1=31 MUXes.

Q34. If S1S0=11 in a 4-to-1 MUX, selected input is:

A) I0

B) I1

C) I2

D) I3

Answer: D) I3
Solution: Binary 11 selects input I3.

Q35. A 1-to-32 DEMUX requires:

A) 4 select lines

B) 5 select lines

C) 6 select lines

D) 32 select lines

Answer: B) 5 select lines
Solution: 2^5=32.

Q36. A 5-to-32 decoder requires:

A) 5 inputs and 32 outputs

B) 32 inputs and 5 outputs

C) 5 inputs and 5 outputs

D) 10 inputs and 32 outputs

Answer: A) 5 inputs and 32 outputs
Solution: Five input bits can select 32 outputs.

Q37. A decoder can be used to generate:

A) Minterms

B) Clock only

C) Analog signals

D) Memory refresh

Answer: A) Minterms
Solution: Each decoder output can represent a minterm.

Q38. A 3-to-8 decoder has how many enable inputs in the simplest basic form?

A) 0

B) 1

C) 3

D) 8

Answer: B) 1
Solution: A common basic decoder has one enable input.

Q39. A priority encoder with 16 inputs requires how many output bits?

A) 2

B) 3

C) 4

D) 8

Answer: C) 4
Solution: 2^4=16.

Q40. A decoder is fundamentally a:

A) Sequential circuit

B) Combinational circuit

C) Memory circuit

D) Oscillator

Answer: B) Combinational circuit
Solution: Decoder output depends only on current inputs.

Flip-Flops & Excitation

Q41. For a JK flip-flop, J=1 and K=0 causes:

A) Hold

B) Reset

C) Set

D) Toggle

Answer: C) Set
Solution: J=1,K=0 sets the flip-flop.

Q42. For a JK flip-flop, J=0 and K=1 causes:

A) Set

B) Reset

C) Toggle

D) Hold

Answer: B) Reset
Solution: J=0,K=1 resets it.

Q43. For a T flip-flop, T=0 causes:

A) Toggle

B) Hold

C) Set

D) Reset

Answer: B) Hold
Solution: T=0 means no change.

Q44. For a D flip-flop, if D=1 immediately before the active edge, Q becomes:

A) 0

B) 1

C) Toggle

D) Invalid

Answer: B) 1
Solution: The next state equals D.

Q45. An SR flip-flop using NOR gates has invalid condition:

A) S=0,R=0

B) S=1,R=0

C) S=0,R=1

D) S=1,R=1

Answer: D) S=1,R=1
Solution: Both inputs high are invalid for a NOR SR latch.

Q46. The excitation inputs required for a JK flip-flop to change from 0 to 1 are:

A) J=0,K=0

B) J=0,K=1

C) J=1,K=X

D) J=X,K=1

Answer: C) J=1,K=X
Solution: J must be 1; K is don't-care.

Q47. For transition 1→0 in a T flip-flop:

A) T=0

B) T=1

C) T=X

D) T=2

Answer: B) T=1
Solution: T=1 toggles 1 to 0.

Q48. To convert a JK flip-flop into a T flip-flop:

A) J=K=T

B) J=T,K=0

C) J=0,K=T

D) J=T',K=T

Answer: A) J=K=T
Solution: Connecting J and K to T gives T-FF behavior.

Q49. To make a D flip-flop operate as a divide-by-2 circuit:

A) D=0

B) D=1

C) D=Q'

D) D=Q

Answer: C) D=Q'
Solution: D=Q' causes Q to toggle each active clock.

Q50. A T flip-flop operating with T=1 behaves as:

A) Frequency doubler

B) Frequency divider by 2

C) Frequency divider by 4

D) Frequency multiplier

Answer: B) Frequency divider by 2
Solution: Every clock toggles Q, so output frequency is f/2.

Timing & Sequential Logic

Q51. If a flip-flop has setup time 5 ns and hold time 3 ns, data must remain stable around the clock edge for at least:

A) 2 ns

B) 3 ns

C) 5 ns

D) 8 ns total interval

Answer: D) 8 ns total interval
Solution: The required stable window spans setup plus hold: 5+3=8 ns.

Q52. Metastability is most closely associated with violation of:

A) Fan-out

B) Setup/hold requirements

C) K-map grouping

D) Decoder operation

Answer: B) Setup/hold requirements
Solution: Setup/hold violations can produce metastability.

Q53. A negative-edge triggered flip-flop responds on:

A) 0→1

B) 1→0

C) 0→0

D) 1→1

Answer: B) 1→0
Solution: Negative edge is a falling transition.

Q54. If the propagation delay through each stage is 12 ns, the approximate delay through five cascaded ripple stages is:

A) 12 ns

B) 24 ns

C) 48 ns

D) 60 ns

Answer: D) 60 ns
Solution: Approximate cumulative delay=5×12=60 ns.

Q55. Clock skew is especially important in:

A) Synchronous systems

B) Pure combinational gates only

C) Resistors

D) Analog filters only

Answer: A) Synchronous systems
Solution: Clock arrival differences affect synchronous timing.

Registers & Shift Operations

Q56. A 12-bit SIPO register needs:

A) 6 flip-flops

B) 8 flip-flops

C) 12 flip-flops

D) 24 flip-flops

Answer: C) 12 flip-flops
Solution: One flip-flop stores one bit.

Q57. A 4-bit register initially contains 1011. After one right shift with serial input 0, the result is:

A) 0110

B) 0101

C) 1101

D) 1010

Answer: A) 0110
Solution: Assuming conventional right shift toward LSB: 1011→0101. Therefore the mathematically correct option is B.

Q58. A 4-bit register initially contains 1011. After one left shift with serial input 0, the result is:

A) 0110

B) 1010

C) 0111

D) 1100

Answer: A) 0110
Solution: Assuming conventional left shift toward MSB with 0 entering LSB: 1011→0110.

Q59. A universal shift register can be used as:

A) Serial-to-parallel converter

B) Parallel-to-serial converter

C) Both A and B

D) Neither

Answer: C) Both A and B
Solution: Universal shift registers support both operations.

Q60. A shift register is fundamentally constructed using:

A) Flip-flops

B) Comparators

C) Decoders only

D) Adders only

Answer: A) Flip-flops
Solution: Each stage is a storage flip-flop.

Advanced Counters

Q61. A 5-bit binary counter is clocked at 32 MHz. The MSB frequency is:

A) 16 MHz

B) 8 MHz

C) 2 MHz

D) 1 MHz

Answer: D) 1 MHz
Solution: Five divide-by-2 stages give 32/32=1 MHz.

Q62. A MOD-20 counter requires minimum:

A) 4 flip-flops

B) 5 flip-flops

C) 6 flip-flops

D) 20 flip-flops

Answer: B) 5 flip-flops
Solution: 2^4=16<20 and 2^5=32≥20.

Q63. A MOD-50 counter requires minimum:

A) 5 flip-flops

B) 6 flip-flops

C) 7 flip-flops

D) 8 flip-flops

Answer: B) 6 flip-flops
Solution: 2^5=32<50 and 2^6=64≥50.

Q64. A 7-bit counter has:

A) 64 states

B) 100 states

C) 128 states

D) 256 states

Answer: C) 128 states
Solution: 2^7=128.

Q65. A MOD-100 counter requires minimum:

A) 6 flip-flops

B) 7 flip-flops

C) 8 flip-flops

D) 10 flip-flops

Answer: C) 8 flip-flops
Solution: 2^7=128 is the first power of 2 at least 100.

Q66. A decade counter implemented using four flip-flops has:

A) 4 unused states

B) 6 unused states

C) 8 unused states

D) 10 unused states

Answer: B) 6 unused states
Solution: 16 total states−10 used=6 unused.

Q67. A ring counter with 8 flip-flops normally has:

A) 8 states

B) 16 states

C) 64 states

D) 256 states

Answer: A) 8 states
Solution: A standard ring counter has n states.

Q68. An 8-bit Johnson counter has:

A) 8 states

B) 16 states

C) 64 states

D) 256 states

Answer: B) 16 states
Solution: Johnson counter has 2n states.

Q69. A counter that counts 0 through 9 and repeats is:

A) MOD-8

B) MOD-9

C) MOD-10

D) MOD-16

Answer: C) MOD-10
Solution: There are ten states.

Q70. The maximum frequency of a ripple counter is mainly limited by:

A) Number of inputs

B) Accumulated propagation delay

C) Number of outputs

D) Memory capacity

Answer: B) Accumulated propagation delay
Solution: Ripple delay accumulates through stages.

Counter Design & FSM

Q71. A synchronous MOD-6 counter requires minimum:

A) 2 flip-flops

B) 3 flip-flops

C) 4 flip-flops

D) 6 flip-flops

Answer: B) 3 flip-flops
Solution: 2^3=8 states are available.

Q72. A MOD-9 counter requires:

A) 3 flip-flops

B) 4 flip-flops

C) 5 flip-flops

D) 9 flip-flops

Answer: B) 4 flip-flops
Solution: 2^3=8<9, so 4 are needed.

Q73. A counter has six valid states. Its modulus is:

A) 3

B) 5

C) 6

D) 8

Answer: C) 6
Solution: MOD equals number of states in the repeating sequence.

Q74. A state machine with 12 states requires minimum state bits:

A) 3

B) 4

C) 5

D) 12

Answer: B) 4
Solution: 2^3=8<12; 2^4=16.

Q75. A Moore machine output changes primarily with:

A) State transitions

B) Input voltage only

C) Memory address only

D) MUX select only

Answer: A) State transitions
Solution: Moore output depends on state; it changes when state changes.

Memory & PLD

Q76. A 16K × 8 memory requires:

A) 8 address lines

B) 12 address lines

C) 14 address lines

D) 16 address lines

Answer: C) 14 address lines
Solution: 16K=2^14.

Q77. A 32K × 16 memory has total capacity:

A) 32 KB

B) 64 KB

C) 128 KB

D) 256 KB

Answer: B) 64 KB
Solution: 32K words×16 bits = 64K bytes=64 KB.

Q78. To build a 16K × 8 memory using 4K × 8 chips, number of chips required is:

A) 2

B) 4

C) 8

D) 16

Answer: B) 4
Solution: 16K/4K=4 chips.

Q79. To build 2K × 16 using 2K × 4 memory chips, number of chips required is:

A) 2

B) 4

C) 8

D) 16

Answer: B) 4
Solution: 16/4=4 chips in parallel.

Q80. Which memory is normally fastest among these?

A) DRAM

B) SRAM

C) Flash

D) ROM

Answer: B) SRAM
Solution: SRAM is generally faster than DRAM.

Q81. Which memory must be refreshed periodically?

A) SRAM

B) DRAM

C) EEPROM

D) Flash

Answer: B) DRAM
Solution: DRAM stores charge in capacitors.

Q82. A 20-bit address bus can address a maximum of:

A) 1 MB

B) 2 MB

C) 4 MB

D) 20 MB

Answer: A) 1 MB
Solution: For byte-addressable memory, 2^20 bytes=1 MB.

Q83. PLA differs from PAL mainly because:

A) PLA has programmable AND and OR arrays

B) PAL has programmable AND and OR arrays

C) PLA has no OR array

D) PAL has no AND array

Answer: A) PLA has programmable AND and OR arrays
Solution: PLA has programmable AND and OR planes.

Q84. FPGA is best described as:

A) Fixed logic circuit

B) Field-programmable digital logic device

C) Analog memory

D) Only a ROM

Answer: B) Field-programmable digital logic device
Solution: FPGA logic can be configured after manufacturing.

Q85. EEPROM differs from traditional EPROM because EEPROM:

A) Cannot be erased

B) Is electrically erasable

C) Requires UV light

D) Is volatile

Answer: B) Is electrically erasable
Solution: EEPROM is electrically erasable.

Logic Families & Performance

Q86. CMOS generally has:

A) High static power

B) Low static power

C) Zero input impedance

D) No noise margin

Answer: B) Low static power
Solution: CMOS has very low static power in steady state.

Q87. Fan-out indicates:

A) Number of inputs

B) Number of loads driven

C) Number of outputs

D) Propagation delay

Answer: B) Number of loads driven
Solution: Fan-out is output load-driving capability.

Q88. If VOH(min)=2.7 V and VIH(min)=2.0 V, the high-level noise margin is:

A) 0.5 V

B) 0.7 V

C) 1.0 V

D) 2.0 V

Answer: B) 0.7 V
Solution: NMH=VOH(min)–VIH(min)=0.7 V.

Q89. If VIL(max)=0.8 V and VOL(max)=0.3 V, the low-level noise margin is:

A) 0.3 V

B) 0.5 V

C) 0.8 V

D) 1.1 V

Answer: B) 0.5 V
Solution: NML=VIL(max)–VOL(max)=0.5 V.

Q90. Power-delay product is measured in:

A) Volt

B) Ampere

C) Joule

D) Ohm

Answer: C) Joule
Solution: Power (W)×time (s)=Joule.

ADC, DAC & Error Detection

Q91. An ideal 12-bit ADC provides:

A) 1024 levels

B) 2048 levels

C) 4096 levels

D) 8192 levels

Answer: C) 4096 levels
Solution: 2^12=4096.

Q92. For a 10-bit ADC with 5 V reference, approximate LSB size is:

A) 1.22 mV

B) 4.88 mV

C) 9.76 mV

D) 10 mV

Answer: B) 4.88 mV
Solution: 5/1024≈4.88 mV.

Q93. A 3-bit ADC has how many quantization levels?

A) 3

B) 6

C) 8

D) 16

Answer: C) 8
Solution: 2^3=8.

Q94. Increasing ADC bits from 8 to 12 increases the number of levels by:

A) 2 times

B) 4 times

C) 8 times

D) 16 times

Answer: D) 16 times
Solution: 2^12/2^8=2^4=16.

Q95. A DAC with more bits generally provides:

A) Lower resolution

B) Higher resolution

C) No output

D) Fewer levels

Answer: B) Higher resolution
Solution: More bits provide finer output steps.

Q96. A code has minimum Hamming distance 5. Maximum number of errors it can correct is:

A) 1

B) 2

C) 3

D) 4

Answer: B) 2
Solution: t=floor((5–1)/2)=2.

Q97. A code with minimum Hamming distance 4 can detect up to:

A) 2 errors

B) 3 errors

C) 4 errors

D) 1 error

Answer: B) 3 errors
Solution: It can detect up to dmin–1=3 errors.

Q98. XOR of 101101 and 110011 is:

A) 011110

B) 001111

C) 111111

D) 010101

Answer: A) 011110
Solution: Bitwise XOR gives 011110.

Q99. A 4-bit binary number has maximum unsigned decimal value:

A) 7

B) 8

C) 15

D) 16

Answer: C) 15
Solution: Maximum = 2^4–1=15.

Q100. A 4-bit 2's-complement system has the decimal range:

A) –7 to +7

B) –8 to +7

C) –15 to +15

D) 0 to 15

Answer: B) –8 to +7
Solution: Range = –2^3 to 2^3–1 = –8 to +7.